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Data Analysis of Manufacturing Test Results for DRAM Module

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What Wiwynn Does?

Solid domain knowledge and experiences + data scientists

Failure Rates with Different DIMM Sizes

3 Million DIMMs

		M1	M2	M3
32GB	Test Qty	1M-2M	0.1M-0.5M	0.1M-0.5M
	Failure rate	0.12%	0.15%	0.06%
16GB	Test Qty	0.1M-0.5M	N/A	<0.1M
	Failure rate	0.07%	N/A	0.08%
8GB	Test Qty	0.1M-0.5M	0.1M-0.5M	0.1M-0.5M
	Failure rate	0.06%	0.07%	0.05%

Failure Rates with Flash Storage

Over 770k Modules

	F1	F2	F3	F4	F5
Test Qty	>10K	>400K	>50K	>50K	>100K
Failure rate	0.08%	0.11%	0.10%	0.14%	0.05%

Failure Rates with Hard Disks

Over 2million Hard Disks

	D1	D2	D2
Test Qty	0.5M-1M	1M-2M	<0.1M
Failure rate	0.07%	0.042%	0.039%

Reliability Engineering of DIMMs

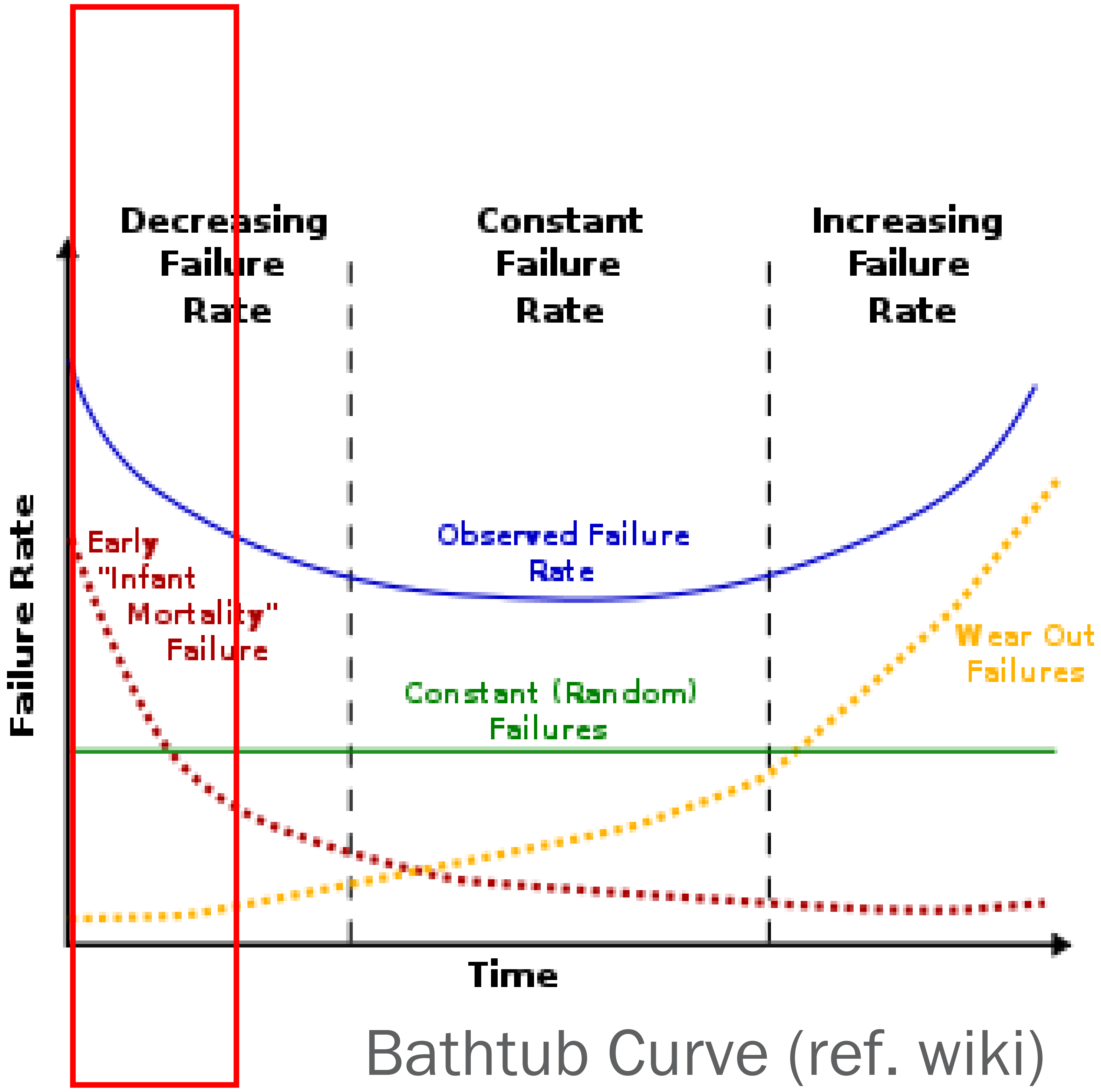
Great impact and difficult to control in production test:

- Difficult to define the golden testing time
- To define the error threshold in the testing time is an open problem
- Require several testing to confirm the defect DIMM modules.

The Stress Test Process for DIMMs

Software

- Run utility to test DIMMs and save logs to SEL (system event log) if any ECC error occurred.
- STRESSAPPTEST version 1.0.3_autoconf, 64 bit binary, Resource: opensource.google.com



Bathtub Curve (ref. wiki)

Testing Model

Variables and Criteria

- Check error-correcting code (ECC) errors in system events log (SEL)

- Testing Time: t_d (ex. 12 hours)
- Correctable ECC error threshold: E_{max} (ex. 6)

- Not Defect DIMM
  - No uncorrectable ECC errors
  - Less than E_{max} errors in total testing time t_d

Data Observation

Dataset

- We test over 80K DIMMs installed on 10K systems in a limit time period

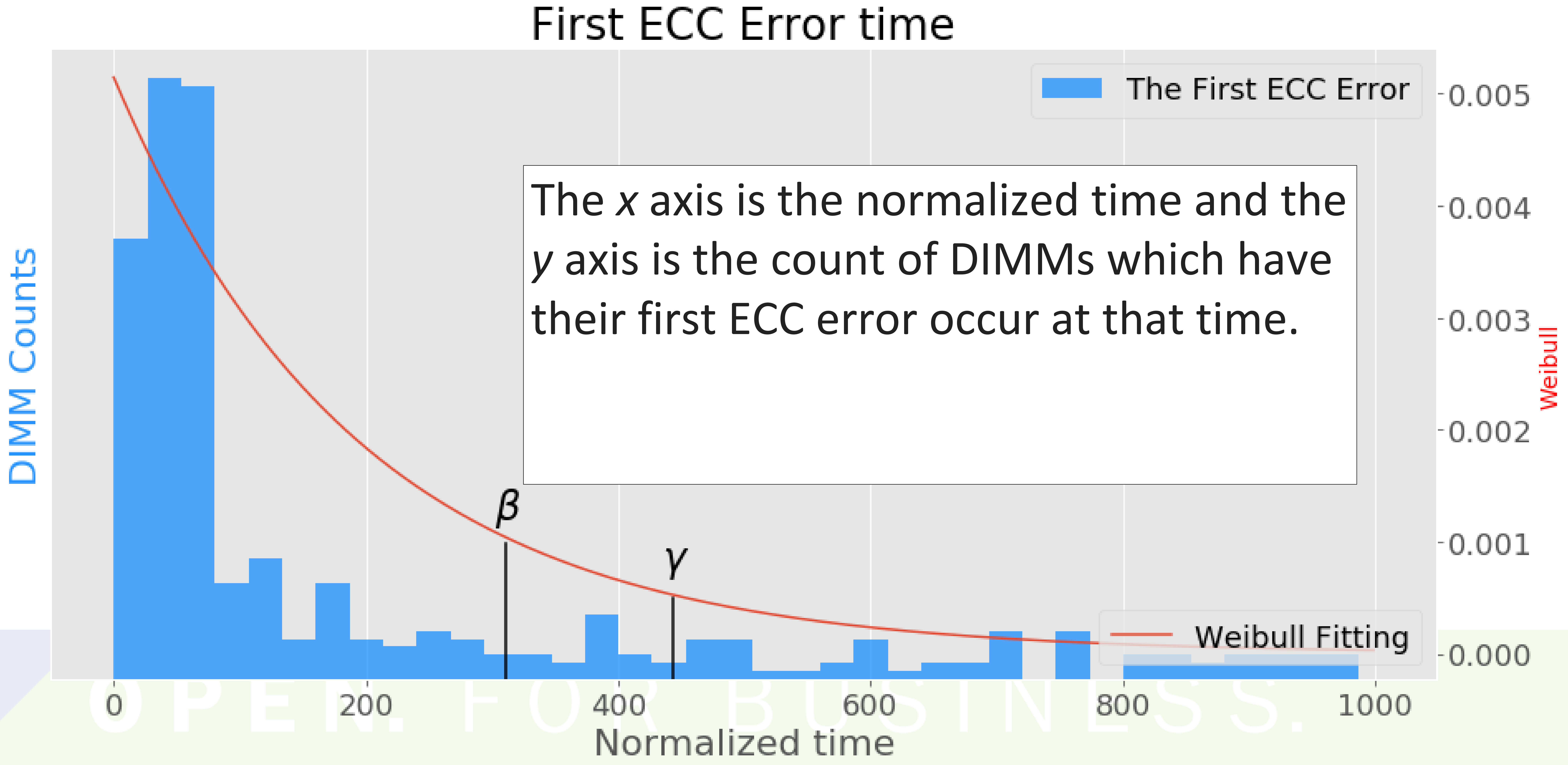
Preliminary Observation of DIMMs Quality

- At least one ECC error occurred in testing

Vendors	A	B	C
ECC Error Rate	0.43%	0.50%	0.30%

Data Observation

Time Distribution of The First ECC Error



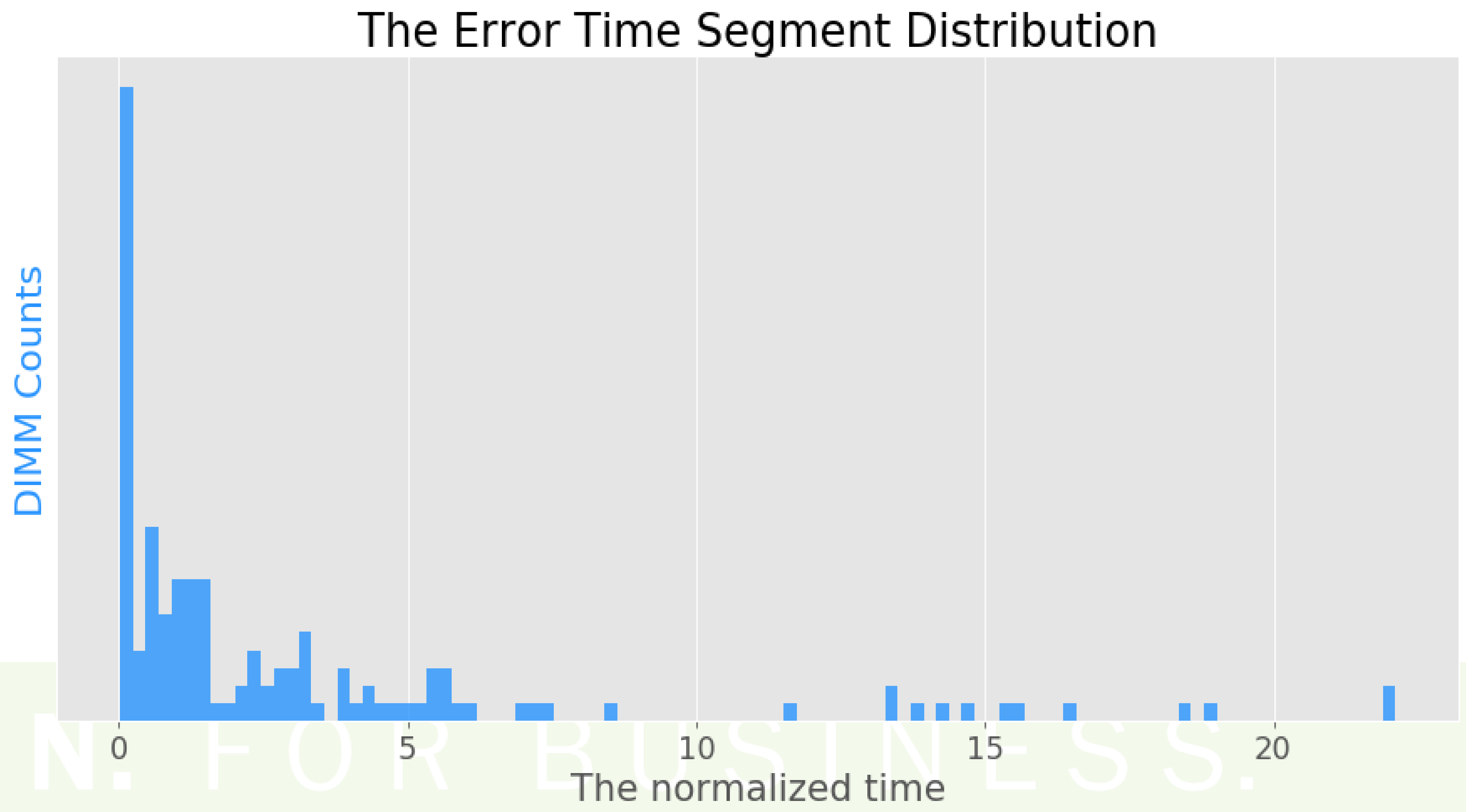
Data Observation

Dataset

- We normalized the total test time in field to 1000 time units for this analysis.
- At least one ECC error in testing
- In limit testing time data, Weibull distribution could predict the global coverage rate.
  - β: *80%* coverage at 311 normalized time point
  - γ: *90%* coverage at 444 normalized time point

The Overview of Recurrent ECC Errors

Time segment distribution between 1st ECC and E_{max} th ECC errors (only show < 25 normalized time)

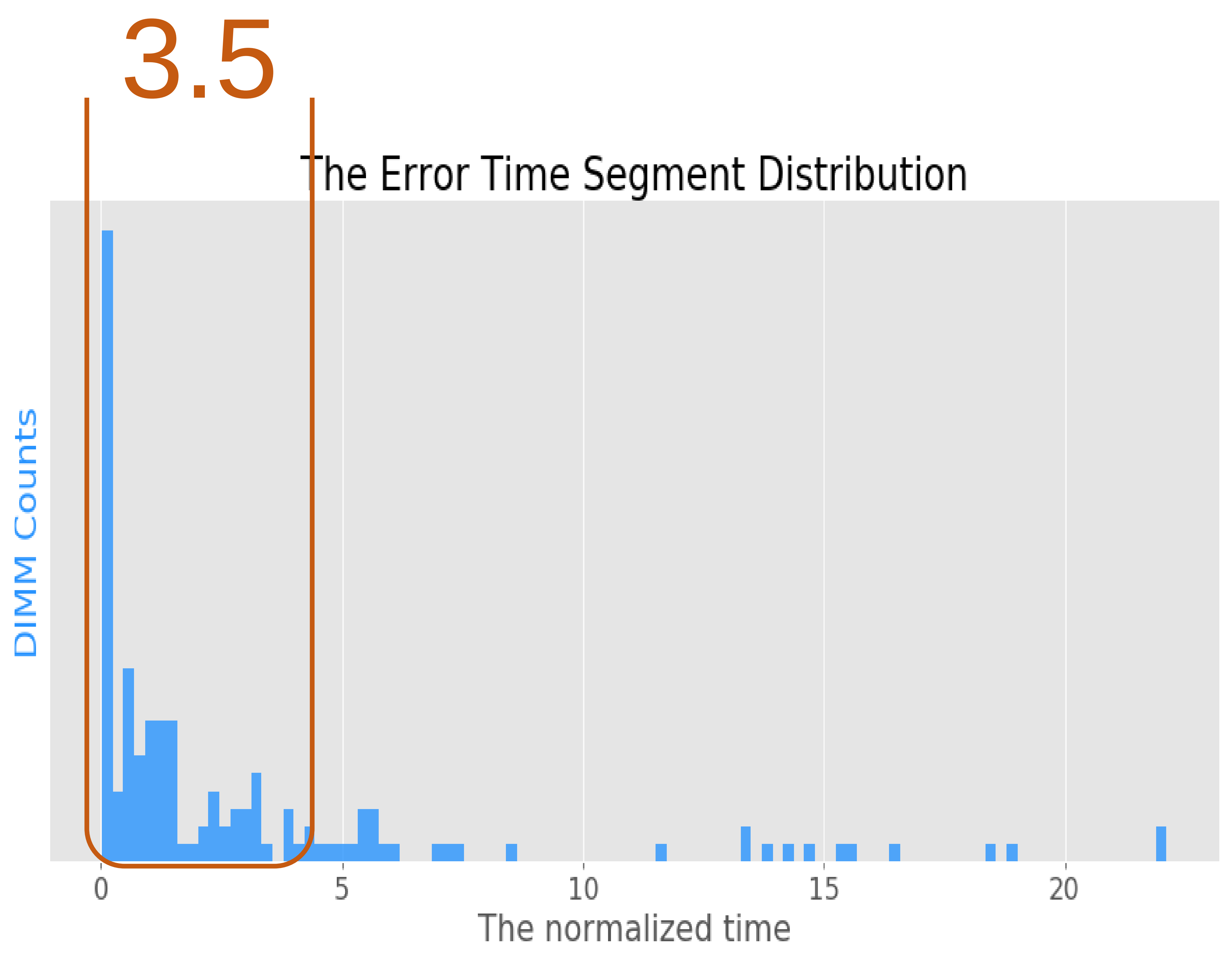


Error Types: Spike and Sparse

The Bucket

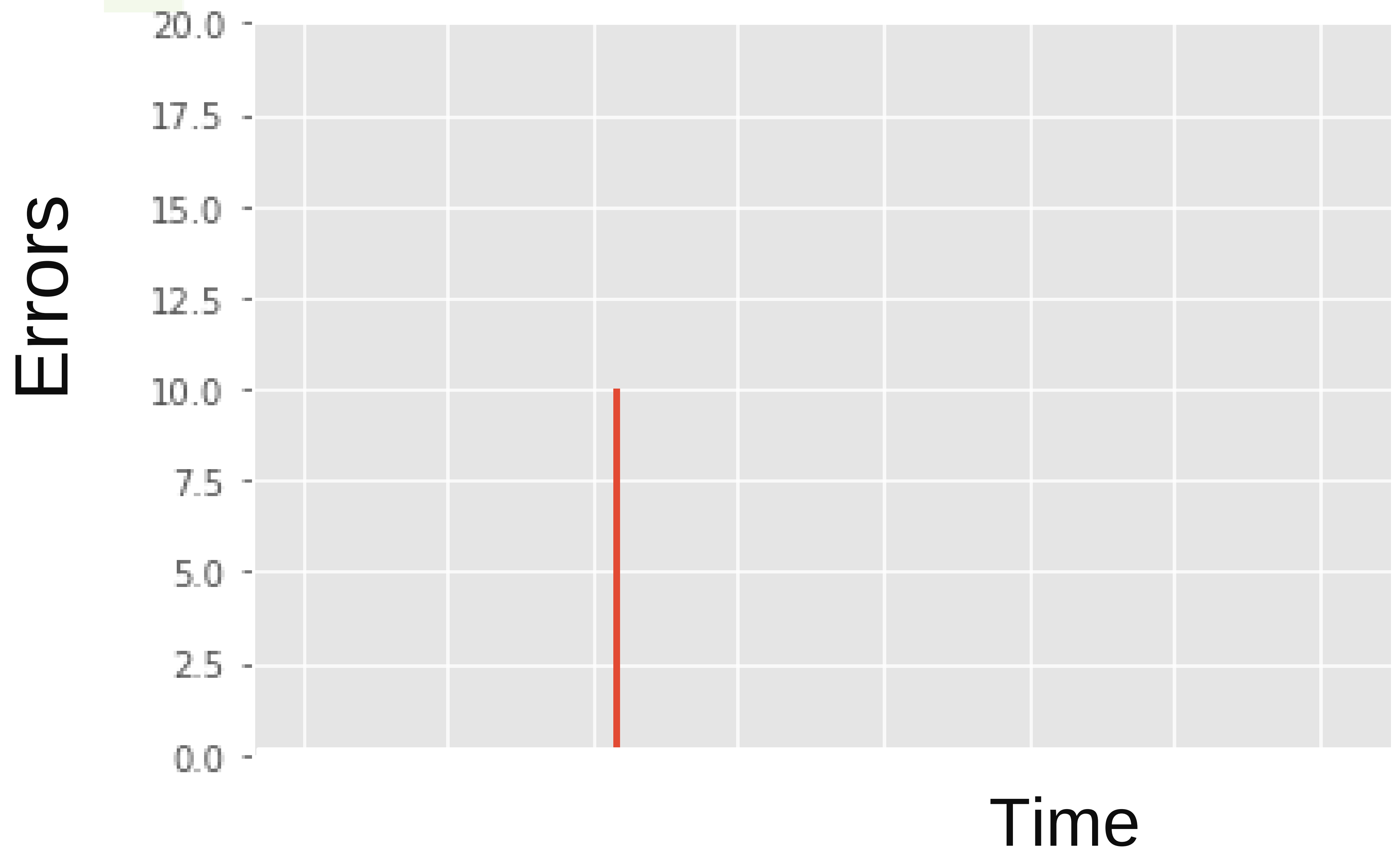
We used the average-linkage hierarchical clustering to analyze the error time segment

A big portion of DIMMs reach their E_{max} th ECC error occurrence within 3.5 normalized time after their first ECC error occurrence.

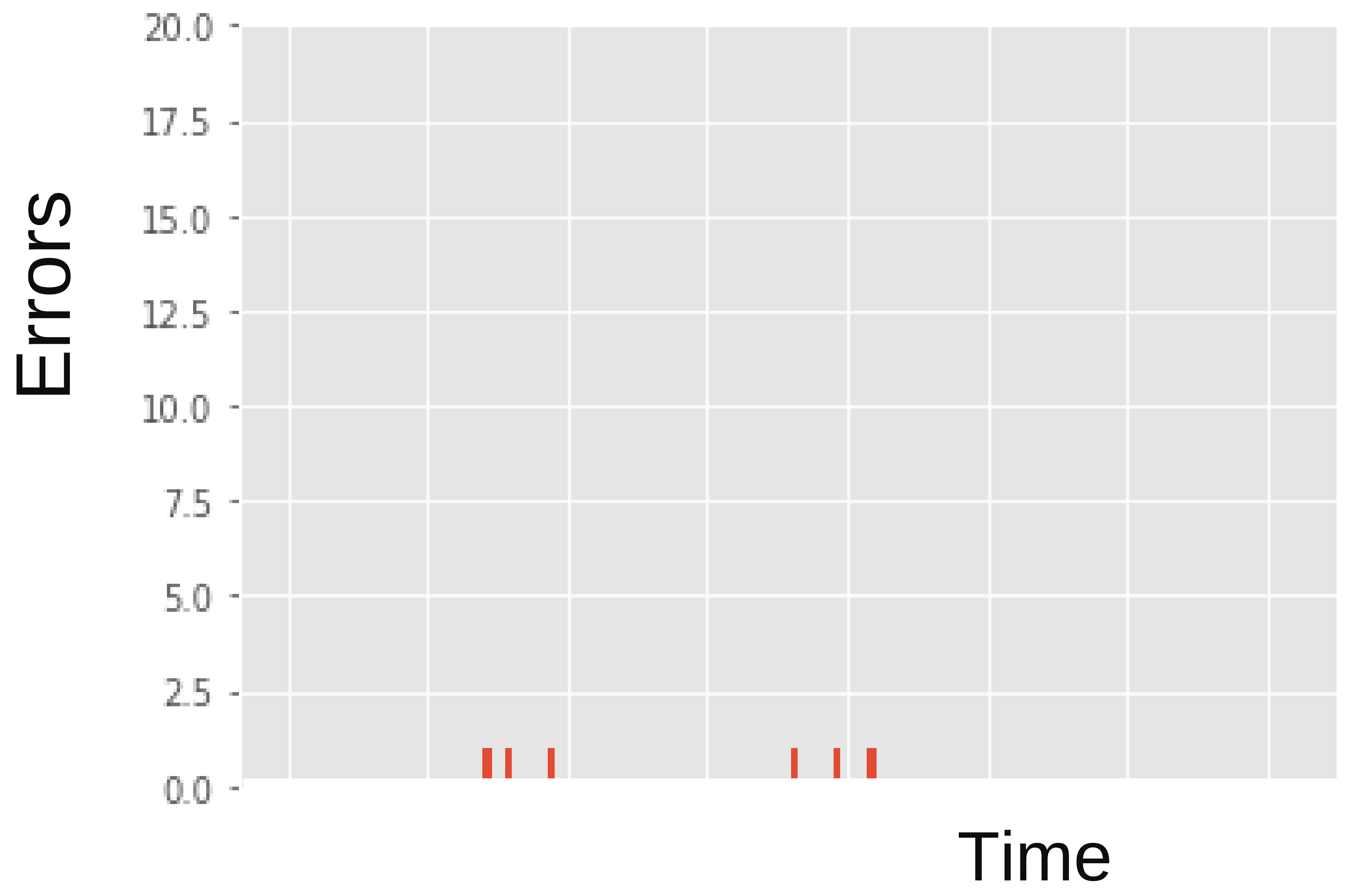


Error Types: Spike and Sparse

The Spike Error Type DIMM

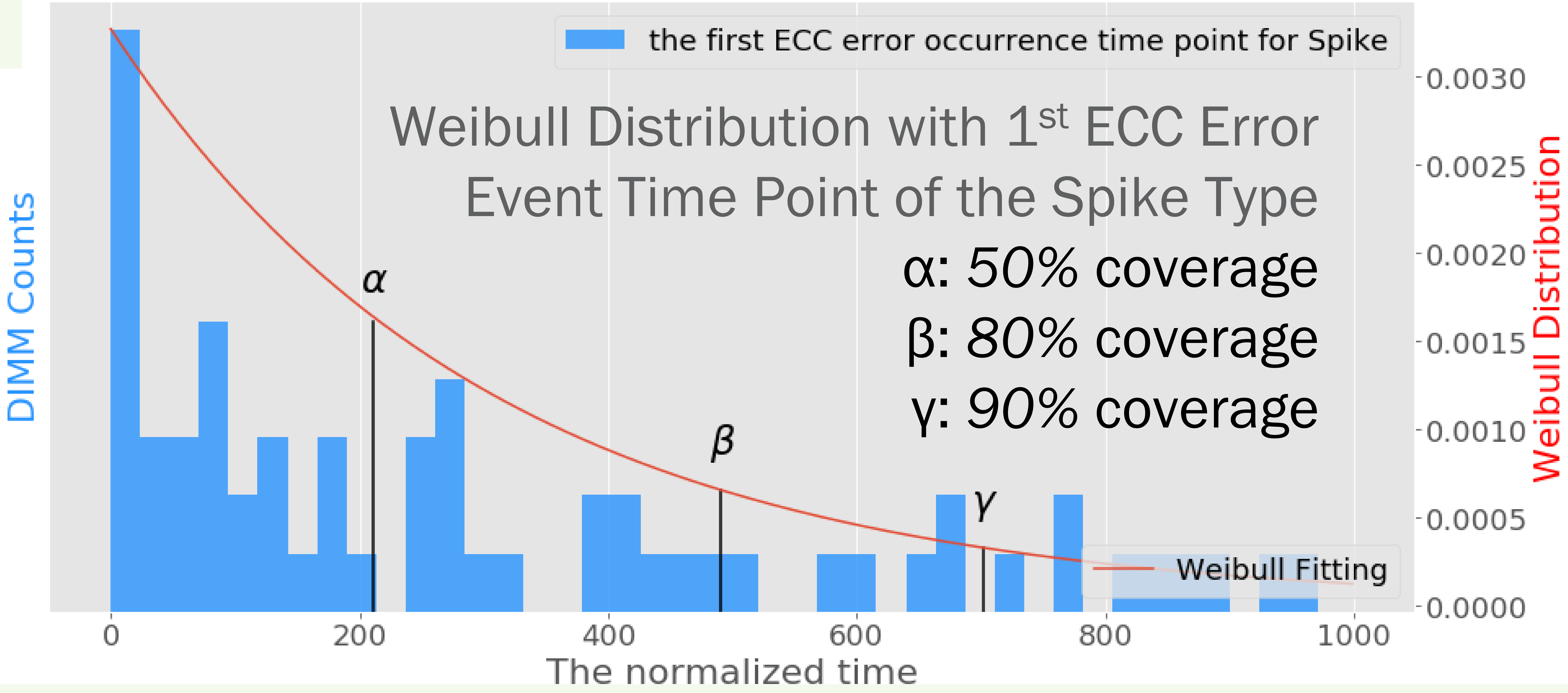


The Sparse Error Type DIMM



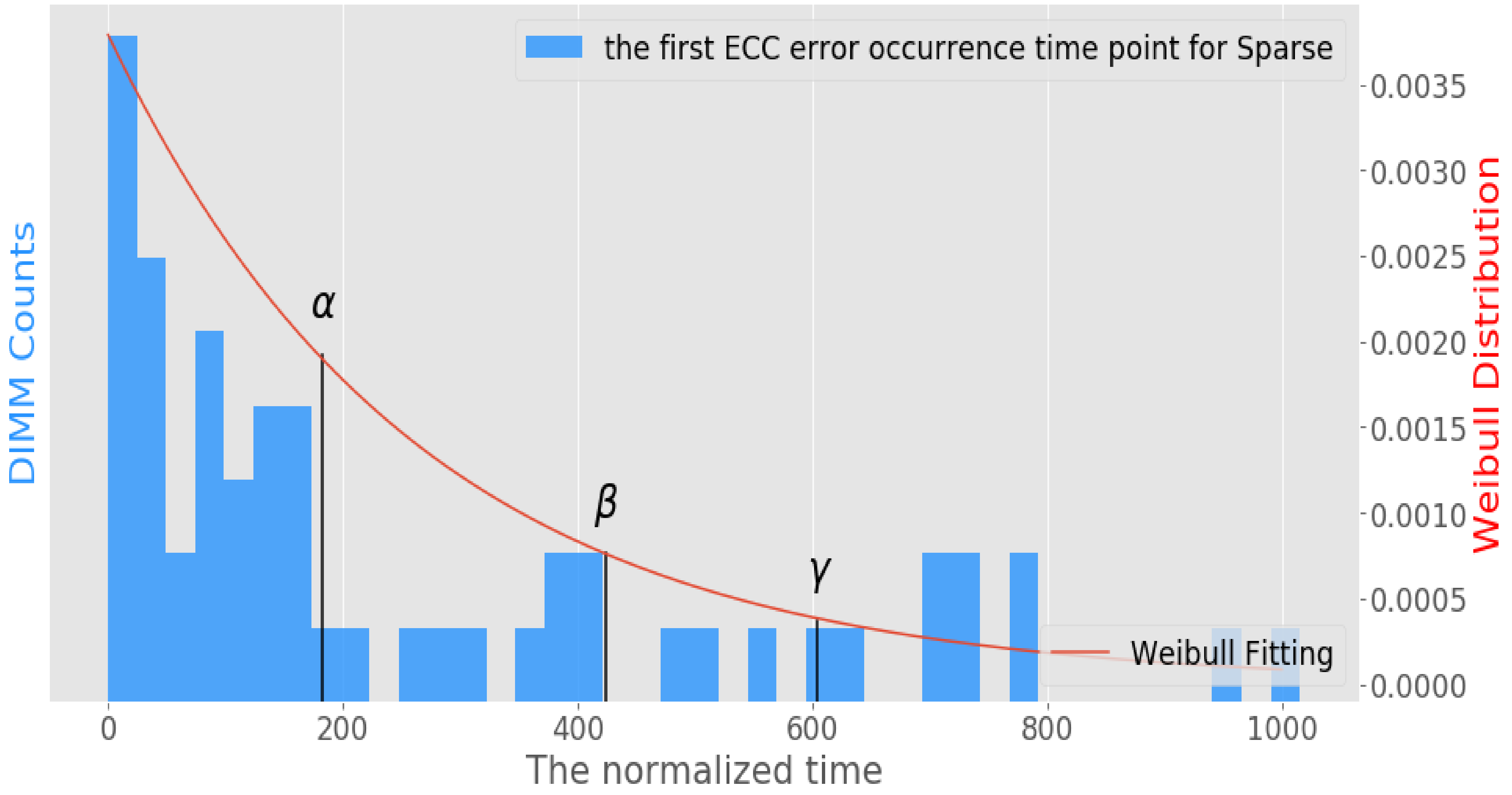
ECC error type	Spike (<=3.5)	Sparse (>3.5)
Percentage	52.55%	47.45%

Spike Assessment

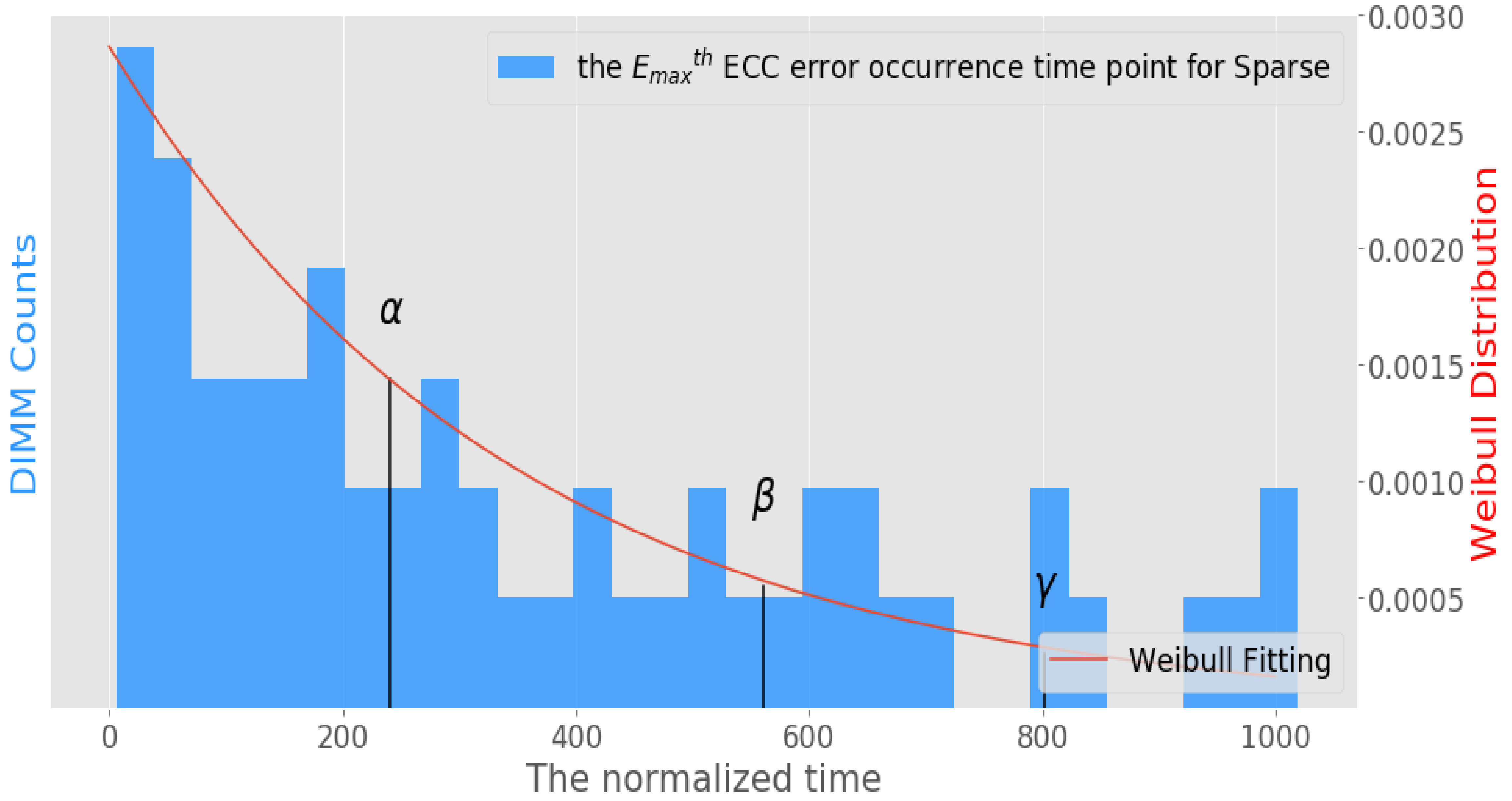


Sparse Assessment

The 1^{st} ECC Error Time Distribution



The $E_{max}{}^{th}$ ECC Error Time Distribution



Weibull Distribution with 1^{st} ECC and $E_{max}{}^{th}$ Error Event Time Point of the Sparse Type

α: *50%* coverage, β: *80%* coverage, γ: *90%* coverage

Our Purpose

Shorten the testing time but maintain quality

It is straightforward to just cut testing time and raise the threshold as compensation.

However, the benefits of less test time will be offset by less error coverage and increased false alarms.

Model Evaluation

Variables and Criteria

- Testing Time, ECC Error Threshold: (t_d , E_{max})
- Defect DIMMs Judged by The Original Criteria (t_d , E_{max}): D_o
- Not Defect DIMMs Judged by The Original Criteria (t_d , E_{max}): N_o

Catch Rate

- (Defect DIMMs Judged by New Criteria and Existed in D_o) / D_o

False Alarm Rate

- (Defect DIMMs Judged by New Criteria and Existed in N_o) / N_o

Analysis of Different Testing Time and ECC error Threshold

Three steps analysis

1. Use trained data (80K) for direct data verification
2. Use the Weibull Distribution to predict criteria
3. Use new data (216K) to cross verify the criteria we predict.

Data Observation – Cross Verification Data

Preliminary Observation of DIMMs Quality

- At least one ECC error in testing (ECC Error Rate)
- More or equal than E_{max} ECC error in the first stress testing (Defect Rate)

Vendors	A	B	C
ECC Error Rate	0.302%	0.302%	0.168%
Defect Rate	0.214%	0.23%	0.107%

Summary

	Catch rate	Testing time	ECC Error threshold	False alarm rate
Direct verification data	90%	0.75 t_d	0.5 E_{max}	0.016%
	80%	0.5 t_d	0.33 E_{max}	0.028%
Cross verification data	90%	0.68 t_d	0.5 E_{max}	0.036%
	80%	0.51 t_d	0.5 E_{max}	0.025%
Prediction based on Weibull distribution	90%	0.7 t_d	0.5 E_{max}	NA
	80%	0.49 t_d	0.5 E_{max}	NA

The Cost-response Model

Elements of The Cost-response Model

1. **Cost with Catch Rate**
    - RMA Costs
    - Operation Loss for External Customer
    - Reputation
2. **Cost with False Alarm Rate**
    - Additional MoH of Testing Time
3. **MoH of Testing Time**

Conclusion

Implement predictive analytics by analyzing event logs generated from the manufacturing process.

Reduce the number of required test and find the best effective stress test time for different parts and brands.

With the optimized test process, we can improve cost and capacity but still keep high quality level.


How Do You Benefits from Data Analysis?
Smart Way to Improve Testing Time and Key Component Quality
Find out more about the manufacturing test results for DRAM Module
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White Paper

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