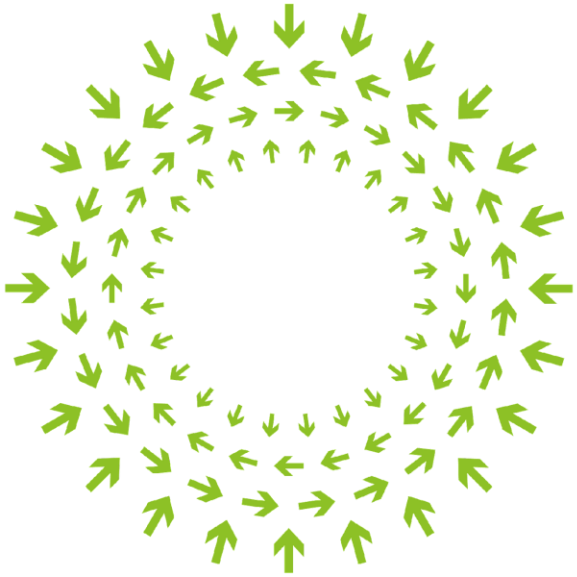

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Compute Project

RunBMC
BMC daughter board I/O specification
Rev1.5 Ver 0.995 Errata

Version 1.0 Revision 1.0 Errata1

Author: Kasper Wszolek, Intel Corporation

Version History

Date	Version #	Author	Description
August 5, 2024	1	Kasper Wszolek (Intel Corporation)	Fix a typo in a signal name listed in Table 6.

Current Template Version:

Specification Errata Template v1.0.0

Effective January 2024

Table of Contents

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2. Acknowledgements

The Contributors of this Specification would like to acknowledge the following for their feedback:

Udo Schmelmer, Kontron Europe GmbH

3. Scope

The purpose of this template is to provide corrections to the following document:
RunBMC BMC daughter board I/O specification Rev1.5 Ver 0.995

4. Errata

List the details of the error and the fixes.

4.1. Issue 1

In the Chapter “5.2.5 VGA/DisplayPort” in the “Table 6 VGA Signals on RunBMC Interface” there’s a typo in the following signal names:

- DACB_NC_DPTXP0
- DACG_NC_DPTXN0

According to the pinout defined in chapter “5.3 Pin Definition” the DACB signal is collocated with DPTXN0 and DACG signal is collocated with DPTXP0. The signal names shall be corrected to:

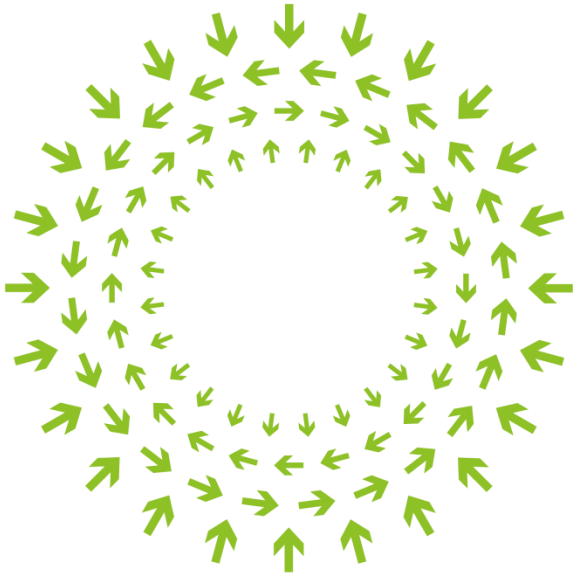
- DACG_NC_DPTXP0
- DACB_NC_DPTXN0

The changes in the “Table 6 VGA Signals on RunBMC Interface” are marked with red color in the Figure 1 below.

Signal Name	Primary Function Description	Secondary Function Description	Tertiary Function Description
DAC~~GB~~_NC_DPTXP0	DAC ~~GB~~ channel output	Not Connected	Display Port Lane 0 (+)
DAC~~BG~~_NC_DPTXN0	DAC ~~BG~~ channel output	Not Connected	Display Port Lane 0 (-)
DACR_NC_DPHPD	DAC R channel output	Not Connected	Display Port Hot Plug Detect
VGAHS_GPIO2_DPTXP1	VGA horizontal sync output	GPIO	Display Port Lane 1 (+)
VGAVS_GPIO4_DPTXN1	VGA vertical sync output	GPIO	Display Port Lane 1 (-)
DDCCLK_GPIO6_DPAUXP	VGA DDC clock pin	GPIO	Display Port Aux Channel (+)
DDCDAT_GPIO8_DPAUXN	VGA DDC data pin	GPIO	Display Port Lane 0 (-)

Table 6 VGA Signals on RunBMC Interface

Figure 1 Issue 1 fix marked in red color.



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Compute Project

RunBMC

BMC daughter board I/O specification
Rev1.5

Authors:
Dropbox: **Eric Shobe**, **Jared Mednick**
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Revision History

Revision	Version	Date	Notes
1.4.1	1.0	Aug 11th 2019	1.0 release
1.5	**0.99**	**Sep 27th 2023**	**Revision 1.5 Candidate:** - **Added support for 6 x I3C interfaces** - **Added support for Display Port output** - **Added RunBMC Power Good indicator (output)** - **Changed CPU_RST# to PLT_RST#** - **Added support for BMC application cores reset**
1.5	**0.995**	**Dec 15th 2023**	- **Editorial fixes and updates**

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2. Table of Contents

3. Scope

This document is a technical specification for the RunBMC used in Open Compute Project. The language used in this document is meant to prescribe a RunBMC module that will conform to this specification. In addition, it provides some recommendations to the design teams of both the module and the system which is expected to receive the module.

4. Overview

This document describes the RunBMC daughter board card design for use with Open Compute Project motherboards. This specification defines the interface between the Baseboard Management Controller (BMC) subsystem and OCP hardware platforms, such as network or compute motherboards.

The RunBMC daughter board interfaces with hardware platforms through a 260 pin SODIMM DDR4 connector, which is intended for mounting into a mating SODIMM DDR4 socket.

Throughout the document, the System on Chip (SoC) which serves the role of Baseboard Management Controller will be referred to as “BMC SoC”. The Daughter Card may be referred to as the RunBMC Module or just “The Module”, with “The Module Designer” Describing the engineering team designing the referred to module. The receiving board will be referred to as “Motherboard / System board” and the engineering team may be referred to as “The Motherboard / System board designer”.

Figure 4-1 shows an example of RunBMC daughter board I/O connectivity

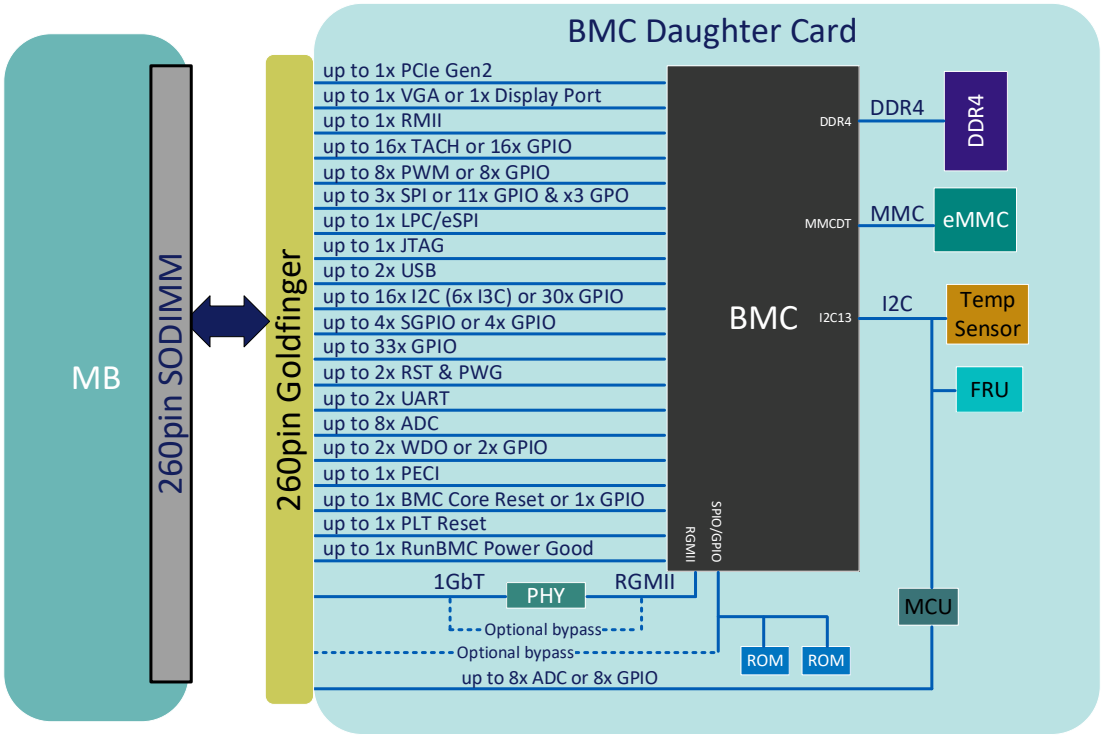


Figure 4-1 An example Block Diagram of BMC Daughter Card with Connector

5. BMC Daughter Board Signaling Interface

5.1 Signal Function Groups

Signal function groups can be summarized in Table 1.

Function	Signal Count for Interface	Number of Interfaces	Number of used pins
Form Factor - 260 SO-DIMM4			
Power 3.3V			5
VDD_RGMII_REF			1
LPC 3.3v or ESPI 1.8v			1
Power 12 V			1
Ground			38
ADC	1	8	8
GPI / ADC	1	8	8
PCIe	7	1	7
RGMII / 1GT PHY	14	1	14
VGA / GPIO / Display Port	7	1	7
RMII / NC-SI	10	1	10
Master JTAG / GPIO	6	1	6
USB host	4	1	4
USB device	3	1	3
SPI1: SPI for host - quad capable	7	1	7
SPI2: SPI for host	5	1	5
FWSPI: SPI for Boot - quad capable	7	1	7
SYSSPI: System SPI	4	1	4
LPC / eSPI	8	1	8
I2C / GPIO	2	8	16
I2C / GPIO / I3C	2	4	8
GPIO / I2C / I3C	2	2	4
GPIO / I2C	2	1	2
I2C	2	1	2
UART (TxD, RxD)	2	4	8
CONSOLE (Tx, Rx)	2	1	2
GPIO / Pass-Through	2	2	4
PWM	1	8	8
Tachometer / GPIO	1	16	16
PECI	2	1	2
GPIO	1	31	31
GPIO / Serial GPIO	4	1	4
Reset and Power Good / GPIO	1	5	3
Watchdog / GPIO	1	2	2
BOOT_IND# / GPIO	1	1	1
RESERVED	1	1	1

Table 1 Count of Signals with Function

5.2 Signal Requirements and Descriptions

The signals are described as a requirement to be provided by the module and are listed as 'The Interface' (shortened from The RunBMC Interface). Motherboard / System designers should consult this document to understand what will be provided by the module and in some cases requirements about components must exist on the receiving board.

A quick note on the naming convention for the signals on the interface. In all cases the functionality provided is the primary information intended to be conveyed by the signal name. The Interface provides many General Purpose Input Output signals, but the numbering may not appear logical. The intention was to number GPIOs to roughly match the physical pin number on the connector, and generally to try to match odd numbered GPIOs to the odd numbered pins, and even numbered GPIOs to the even numbered pins. See Table 26 for more information and complete interface pinout on the 260-pin connector.

5.2.1 Power

For all power requirements (red cells highlighted Table 1), please reference “Electrical and Timing Requirements”.

5.2.2 ADC

The Interface shall provide sixteen voltage sensing channels (Analog-to-Digital Conversion). Eight of these are dedicated with sole functionality as ADC channels. The remaining eight primarily function as GPI (General Purpose Input) but may be configured as ADC if desired. This means that, per signal, these remaining eight signals may be used by the motherboard / system designer exclusively as analog inputs to the RunBMC module or exclusively as digital inputs.

Signal Name	Description, Primary Function	Secondary Function?
ADC[0-7]	Analog-to-Digital Conversion	None (Analog Channels only)
GPI[0-7]_ADC[8-15]	General Purpose Input	Analog-to-Digital Conversion

Table 2 Analog Input Channels on the RunBMC Interface

5.2.3 PCIe

The Interface shall provide a PCIe connection which supports a PCI-Express Gen 2 One Lane (x1) connection. This interface shall be capable of PCI-Express “Endpoint” functionality. These signals are expected to be dedicated to PCIe functionality and should not offer a secondary function.

Signal Name	Description
PERXN	PCI-Express Receive Negative
PERXP	PCI-Express Receive Positive
PETXN	PCI-Express Transmit Negative
PETXP	PCI-Express Transmit Positive
PEREFCLKN	PCI-Express Reference Clock Negative
PEREFCLKP	PCI-Express Reference Clock Positive
PERSTN	PCI-Express Reset Signal, Active-low

Table 3 PCIe signals on the RunBMC Interface

5.2.4 Ethernet and RGMII

The Interface shall allow flexibility for an Ethernet interface as primary function as shown in the Table 4 for “1GbT usage” (i.e., 1000BASE-T or IEEE 802.3ab). Secondary functions on these I/Os allow for a RGMII interface to be routed over the connector if desired as shown in the “RGMII interface” (Reduced Gigabit Media-Independent Interface). This flexible interface also supports Management Interface signals specific to the RGMII (MDC & MDIO).

The RunBMC Interface shall allow designers to use PHYs that have different I/O voltage requirements than what the BMC SoC can drive natively. VDD_RGMII_REF, an output reference

voltage, may be used to accomplish these types of scenarios. Please see section 6 for electrical guidelines. Section 10 highlights platform guidelines and usage for VDD_RGMII_REF signal.

1GbT usage	RGMII usage

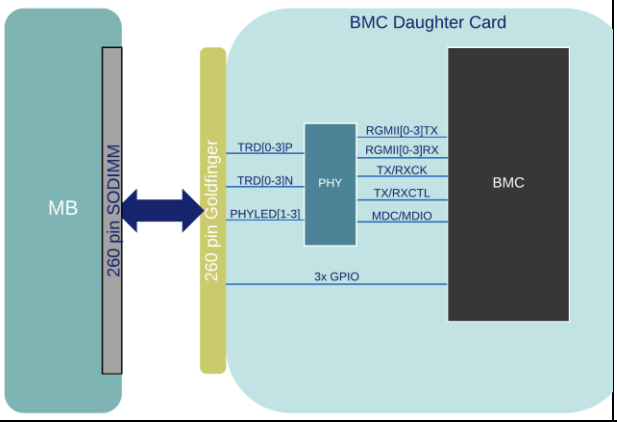
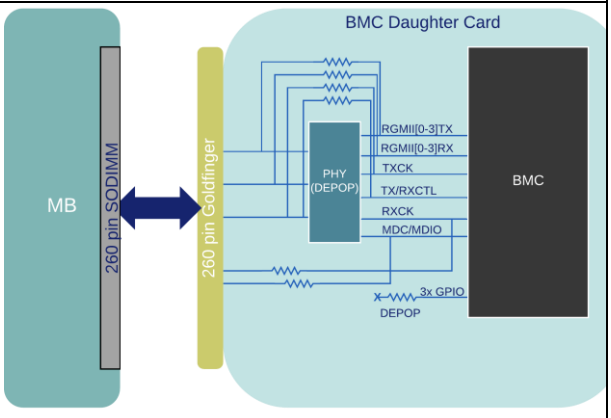

	

Figure 5-1 Showing 1GbT routed over connector	Figure 5-2 Depopulated PHY on module, RGMII over connector. Usage of RGMII on MB not shown.

Table 4 1GbT Interface vs RGMII usage

Signal Name	Primary Function Description	Secondary Function Description
TRD[0-3]P_RGMII[0-3]TX	1000BASE-T Differential Pair Positive	RGMII Transmit
TRD[0-3]N_RGMII[0-3]RX	1000BASE-T Differential Pair Negative	RGMII Receive
PHYLED1_RGMIITXCK	PHY LED Signal 1 (See PHY Datasheet)	RGMII Transmit Clock
PHYLED2_RGMIIRXCTL	PHY LED Signal 2 (See PHY Datasheet)	RGMII Receive Control
PHYLED3_RGMIITXCTL	PHY LED Signal 3 (See PHY Datasheet)	RGMII Transmit Control
GPIO127_RGMIIMDC	General Purpose Input Output	Management Interface Clock Output
GPIO128_RGMIIMDIO	General Purpose Input Output	Management Interface Data Input / Output
GPIO129_RGMIIRXCK	General Purpose Input Output	RGMII Receive Clock

Table 5 Dual Function Ethernet and RGMII Signals on RunBMC Interface

5.2.5 VGA/DisplayPort

The Interface shall provide VGA (Video Graphics Array) or alternatively Display Port functionality with the required signals as listed in Table 6. It is mandatory that, in the case of using the VGA signals or Display Port signals, the motherboard / system designer take care to understand that secondary functions (as GPIO) are not supported.

Signal Name	Primary Function Description	Secondary Function Description	Tertiary Function Description
DACB_NC_DPTXP0	DAC B channel output	Not Connected	Display Port Lane 0 (+)
DACG_NC_DPTXN0	DAC G channel output	Not Connected	Display Port Lane 0 (-)
DACR_NC_DPHPD	DAC R channel output	Not Connected	Display Port Hot Plug Detect
VGAHS_GPIO2_DPTXP1	VGA horizontal sync output	GPIO	Display Port Lane 1 (+)
VGAVS_GPIO4_DPTXN1	VGA vertical sync output	GPIO	Display Port Lane 1 (-)
DDCCLK_GPIO6_DPAUXP	VGA DDC clock pin	GPIO	Display Port Aux Channel (+)
DDCDAT_GPIO8_DPAUXN	VGA DDC data pin	GPIO	Display Port Lane 0 (-)

Table 6 VGA Signals on RunBMC Interface

In case of VGA usage motherboard / system designer should ensure proper RGB terminations and filtering based on RGB trace impedance. Figure 5-1 shows the recommended VGA topology.

Two 150R terminations should be present in VGA trace:

- One 150R should be close to SOC that is on the RunBMC module.
- One 150R should be close to filter on the Motherboard.
- System designers should reference their BMC vendor design guide for further recommendations.

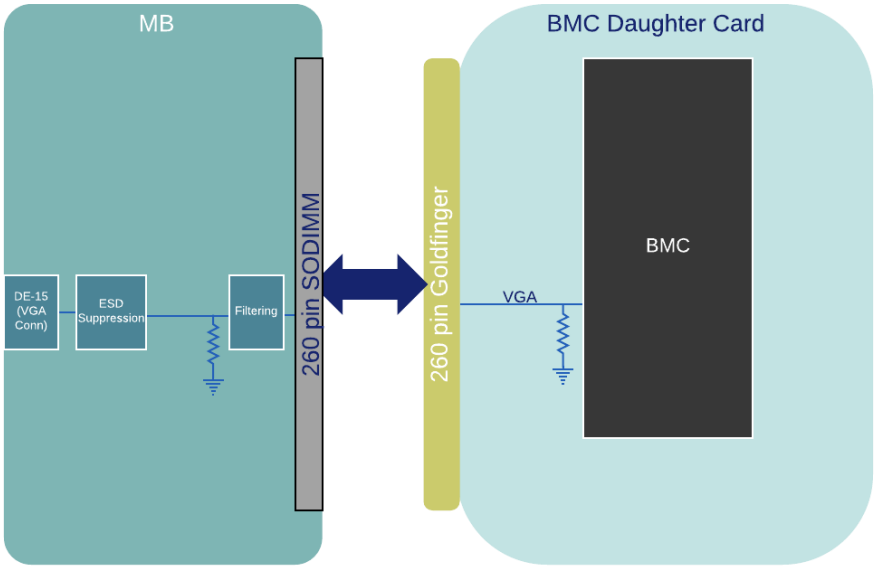


Figure 5-3 Recommended Filtering Topology for VGA

Note: For the Display Port topologies please follow specific Display Port/Mini Display Port connector requirements regarding ESD protection and CMC signal-noise level requirements.

5.2.6 RMII/NCSI

The Interface shall provide a single RMII (Reduced Media Independent Interface) / NC-SI (Network Controller Sideband Interface) flexible interface with ten dedicated pins. MDC and MDIO signals shall also be provided over the connector specific to this interface. These signals are dedicated and will not support a second function.

Signal Name	Description
RMIIRXD[0-1]	RMII / NC-SI Receive Data
RMIITXD[0-1]	RMII / NC-SI Transmit Data
RMIITXEN	RMII / NC-SI Transmit Enable
RMIIRXER	RMII / NC-SI Receive Data Error
RMIIRCLKI	RMII / NC-SI 50 MHz Reference Clock
RMIICRSDV	RMII / NC-SI Carrier Sense / Receive Data Valid
RMIIMDC	RMII Management Interface Clock Output
RMIIMDIO	RMII Management Interface Input / Output

Table 7 Flexible RMII / NC-SI Interface Signals on RunBMC Interface

5.2.7 JTAG

The Interface shall provide a single JTAG, which is meant to act as a master. The typical five signals are defined including RTCK as a sixth signal not typically used in master applications. None of these signals shall support any secondary function.

Signal Name	Description
JTAG1TRST	Defines Test Reset, output from BMC
JTAG1TMS	Test Mode Select, output from BMC
JTAG1TDO	Test Data Out, input to BMC
JTAG1TDI	Test Data In, output from BMC
JTAG1TCK	Test Clock, output from BMC
JTAG1RTCK	Return Test Clock, input to BMC (if used)

Table 8 JTAG Signals on the RunBMC Interface

5.2.8 USB2A Host/Device

The Interface shall provide a USB interface capable of both USB host and USB device functionality, called USB2A. Two additional signals for USB are included, which are recommended to be used exclusively for either host or device functionality. See Table 9 for more details of these additional signals.

Signal Name	Definition	Primary Function Description	Secondary Function Description
USB2A_HD_DN	USB Data Minus	Differential Signal for USB	None
USB2A_HD_DP	USB Data Plus	Differential Signal for USB	None
GPIO125_USB2AVBUSSNS	Device VBUS Sense	GPIO	**Shall be used when BMC SoC acts as USB Device Only.** Detects 5 V supply is asserted and allows the BMC to have its device port begin USB host negotiation. Note that use of the 5 V supply detect is meant to indicate to the BMC as a device that a host is attached and supplying power.
GPIO126_USB2APWREN	Host/device VBUS Control	GPIO	**Shall be used when BMC SoC acts as USB Host Only.** Output to control 5V supply to USB device. In the case that the USB Device attached to the BMC enters an over-current state (as indicated by USB Over Current Sense) the BMC will de-assert this signal and 5 V supply to the USB device will go into a low voltage or low current state, such that the device will no longer have power.

Table 9 USB Host / Device Signals on RunBMC Interface

5.2.9 USB2B Device

The Interface shall provide a second USB interface which needs only to have USB device capability, called USB2B. One additional signal for this interface is provided, which is recommended to be used to sense adding a USB Device.

Signal Name	Definition	Primary Description	Secondary Function Description
USB2B_D_DN	USB Data Minus	Differential Signal for USB	None
USB2B_D_DP	USB Data Plus	Differential Signal for USB	None
GPIO123_USB2BVBUSSNS	Device VBUS Sense	GPIO	Detects 5 V supply is asserted and allows the BMC to have its device port begin USB host negotiation. Note that use of the 5 V supply detect is meant to indicate to the BMC as a device that a host is attached and supplying power.

Table 10 USB Device Signals on RunBMC Interface

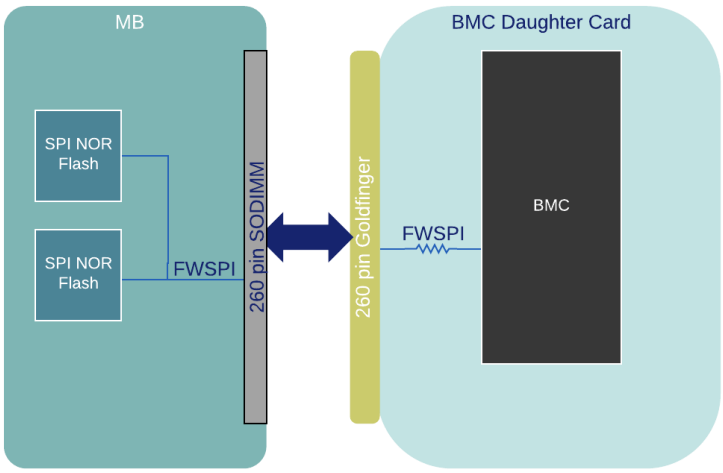
5.2.10 Firmware SPI

The Interface shall provide Firmware SPI for the BMC SoC with the option to depopulate components such that the Firmware SPI bus is not exposed over the Interface. The BMC SoC is a SPI Bus Master to this Bus.

The Firmware Serial Peripheral Interface (FWSPI) bus, which is used by the BMC SoC for boot over NOR Flash, has a dual function as NC, or not connected. The RunBMC specification details three scenarios where the boot flash device may be located: off the module, on the module exposing the FWSPI interface, or on the module without exposing the FWSPI interface (in which case it is NC). RunBMC module designers will provide the ability to provide NC or FWSPI through hardware multiplexing (for example, resistor population options are valid). Table 10 details these options. It is recommended that the motherboard / system designer consult module specific documentation to understand what functionality is provided in this specific case.

The BMC SoC boots from a flash memory device located on the FWSPI bus. The device size is 256Mb (32MB) minimum and can be used to store FPGA, CPLD, and miscellaneous recovery images as well as BMC Firmware. A secondary device is supported to provide BMC recovery and firmware updates, which can be used by the extra chip select, available on the connector.

The RunBMC module may have the Primary & Secondary NOR Flash onboard (Called On-Module Boot Media in Table 11) or utilize the FWSPI signal pins over the connector if placement on the baseboard is mandatory. Refer to Signal Priority and Nomenclature section of this specification.

Figures	Description
 Figure 5-4 Off-Module Boot Media	Scenario 1: The Off-Module Boot Media case uses the FWSPI interface on the connector to route to a SPI NOR Flash boot device that lives on the system board.

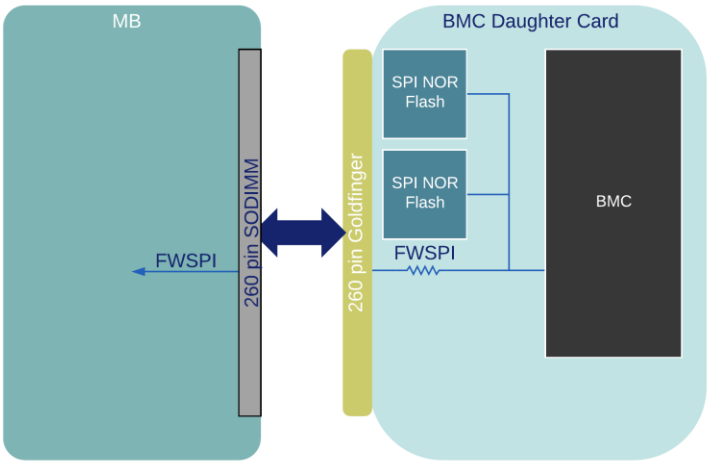


Figure 5-5 On-Module Boot Media with FWSPI bus Exposed over RunBMC interface

Scenario 2: The On-Module Boot Media with FWSPI interface exposed through the connector is shown, with a redundant SPI NOR Flash device. In this case the system board can access the FWSPI interface; this lends itself to use cases such as re-programming the boot flash for the BMC from the system board. Note that connections on the MB are not shown in this diagram.

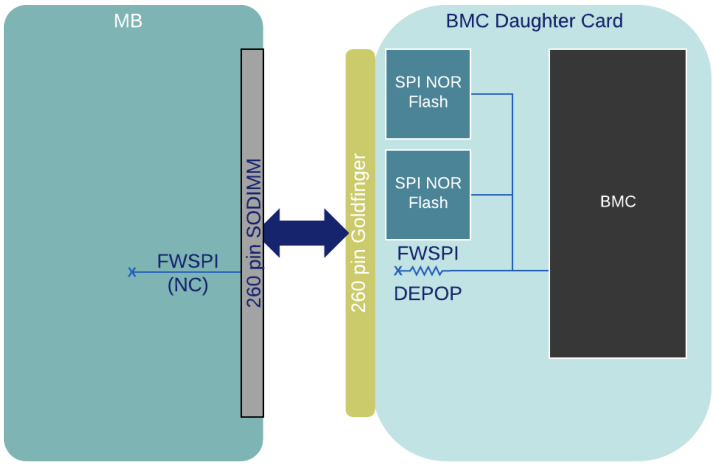


Figure 5-6 Off-Module Boot Media with FWSPI bus isolated from RunBMC interface

Scenario 3: An example of the On-Module Boot Media with FWSPI interface not exposed is shown here, with resistors connecting the FWSPI de-populated. This may be advisable when security concerns necessitate that the BMC should have total control of the FWSPI interface. The diagram is meant to illustrate that the resistor stuffing option has been depopulated, so the FWSPI pins on the motherboard are floating / Not Connected (NC).

Table 11 RunBMC FWSPI topology options

Signal Name	Notes	Primary Description	Secondary Function Description
FWSPICS0#	For Primary Boot Device	Chip Select Zero	None
FWSPIMOSI_IO0	Quad SPI may not be supported	Master Output Slave Input or Input Output 0	None
FWSPIMISO_IO1	Quad SPI may not be supported	Master Input Slave Output or Input Output 1	None
FWSPI_IO2_GPIO41	If NC (Scenario 3 in Table 10), GPIO still provided	Input Output 2	GPIO
FWSPI_IO3_GPIO43	If NC (Scenario 3 in Table 10), GPIO still provided	Input Output 3	GPIO
FWSPICK	Typically generated by BMC SoC	Master Clock	None
FWSPICS1#	For Secondary Boot Device	Chip Select One	None
GPIO35_FWSPIWP#	Write Protect for Boot Device	GPIO	Active-low Write Protect

Table 12 Firmware SPI Signals on RunBMC Interface

5.2.11 SPI Master Interface for Host

Three additional Serial Peripheral Interface (SPI) Master Controller interface signals shall be provided by the Interface. Two busses shall provide two chip selects used to select the primary or secondary SPI Flash device's if used. The remaining bus (SYSSPI) shall only have 1 chip select.

All SPI Host interfaces are multiplexed with GPIOs or GPOs. It is recommended that the motherboard / system designer take special note of which functions are General Purpose Output and, in the case of using for secondary function, should use these signals for output signals from the perspective of the BMC SoC. Note that Quad SPI is supported by the RunBMC interface for some of these SPI Busses, but not guaranteed by the BMC SoC.

SPI	Net Names	Quad SPI (if Supported by BMC SoC)	Number of Chip Selects
Firmware/Boot SPI	FWSPI*	Y	2
Host SPI Interface 1	SPI1*	Y	2
Host SPI Interface 2	SPI2*	N	2
System SPI	SYSSPI*	N	1

Table 13 Overview of SPI busses on RunBMC Connector

SPI	Signal Name	Primary Function Description	Secondary Function Description
Host SPI Interface 1	SPI1CS0#_GPIO116	Chip Select Zero	GPIO
	SPI1MOSI_IO0_GPO3	Master Output Slave Input or Input Output 0	General Purpose Output (GPO, No Input)
	SPI1MISO_IO1_GPO4	Master Input Slave Output or Input Output 1	GPO
	GPO5_SPI1_IO2	Input Output 2	GPO
	GPIO120_SPI1_IO3	Input Output 3	GPO
	SPI1CK_GPIO122	Clock	GPIO
	SPI1CS1#_GPIO124	Chip Select One	GPIO
Host SPI Interface 2	SPI2CK_GPIO78	Clock	GPIO
	SPI2MISO_GPIO80	Master Input Slave Output	GPIO
	SPI2MOSI_GPIO82	Master Output Slave Input	GPIO
	SPI2CS0#_GPIO84	Chip Select Zero	GPIO
	SPI2CS1#_GPIO86	Chip Select One	GPIO
System SPI	SYSCS#_GPIO112	Chip Select	GPIO
	SYSMISO_GPO1	Master Input Slave Output	GPO
	SYSMOSI_GPO2	Master Output Slave Input	GPO
	SYSCK_GPIO114	Clock	GPIO

Table 14 Additional SPI Busses on the RunBMC Interface

5.2.12 LPC/eSPI

The Interface shall provide both a Low Pin Count (LPC) and Enhanced Serial Peripheral Bus (eSPI) combined onto the same physical pins. The RunBMC module designer may choose to multiplex with hardware if software pin multiplexing is not supported between these interfaces on the BMC SoC.
Signal voltage levels are defined by VDD_LPC3V3_ESPI1V8 signal. Please reference section 6 for electrical requirements.

Signal Name	LPC Functionality Description	eSPI Functionality Description
LPCRST#_ESPIRST#	Active-low bus reset input	Active-low bus reset input
LPCD[0-3]_ESPID[0-3]	Address & Data bus bits 0 to 3	Data Bus bits 0 to 3
LPCIRQ#_ESPIALERT#	Serial Interrupt Request Output	Alert Output
LPCFRAME#_ESPICS#	Frame	Chip Select Input
LPCCLK_ESPICLK	Bus Clock Input (33.3 MHz)	Bus Clock Input

Table 15 LPC and eSPI Signals on the RunBMC Interface

5.2.13 I2C/I3C

The Interface shall provide a total of sixteen I2C busses which shall be SMBus compatible 2-wire interfaces consisting of a serial data line (SDA) and a serial clock line (SCL). If the SoC on the daughterboard uses IO cells that are open-drain, the baseboard device shall require a pullup resistor to generate a logic high voltage and shall remain high even when the bus is idle.

I2C Bus 9 is a special-use case bus to provide both a FRU ID EEPROM for RunBMC module identification and the RunBMC SoC should be addressed as a slave on this bus. See Section 9 for more details about the identification EEPROM.

Proper power domain isolation shall be implemented on the daughterboard. The AC/DC specifications are defined in the SMBus 2.0 and I^2C bus specifications.

The I3C interfaces are defined as tertiary functions on existing I2C interfaces. The I3C interfaces are following MIPI I3C Basic 1.1.1 specification. The voltage levels of I3C interfaces on typical server designs are defined at 1.0V and 1.8V while the I2C interfaces defined in RunBMC are set at 3.3V. In order to support backward compatibility with previous RunBMC standards, devices like I3C Hubs shall be used as presented in the Figure 5-7. The I3C Hub can support 1.0V and 1.8V I3C operation as well as 3.3V tolerance for backward compatibility with I2C traffic support. I3C Hub can also provide fanout from single I3C link into multiple links or multiple I3C Hubs can be used.

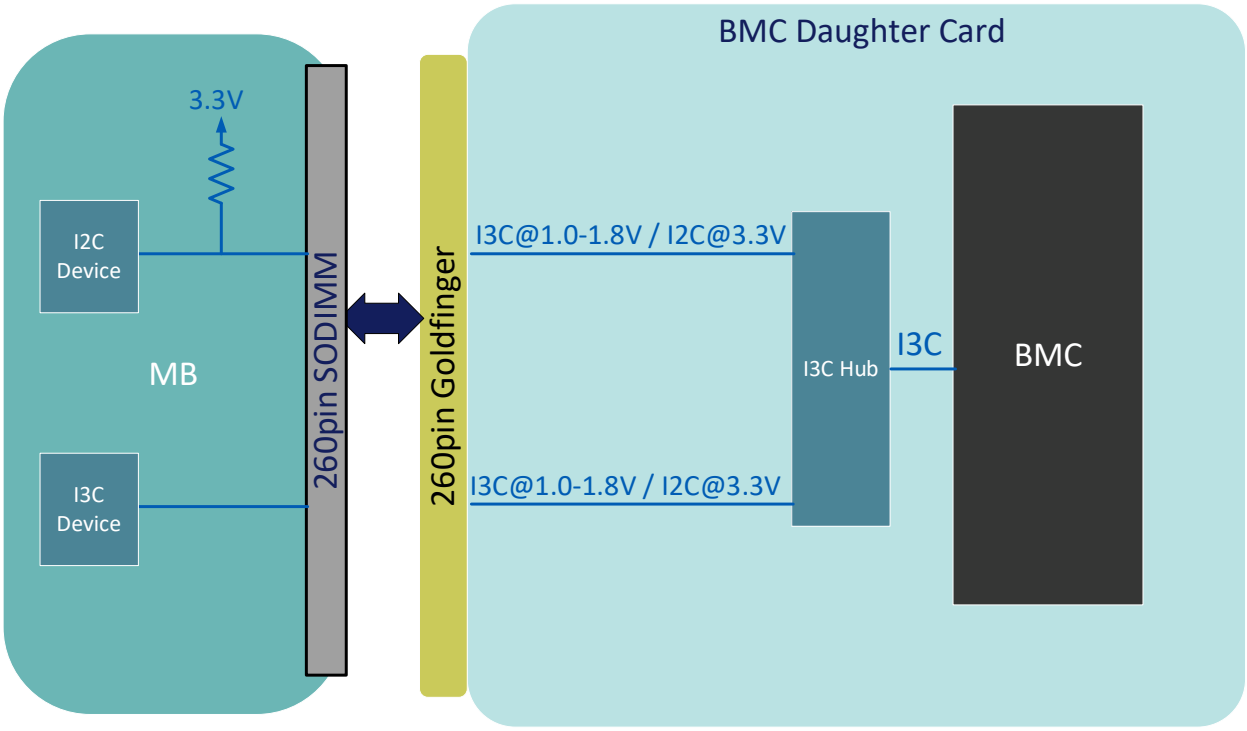


Figure 5-7 Example use of I3C Hub to support I3C at lower voltages and maintain backward compatibility with I2C 3.3V

Note:

1. In designs that do not intend to be backward compatible on I3C links and will only be used with motherboard designs using I3C links, I3C Hubs can be omitted and links can be directly connected to BMC.

2. Other solutions providing backward compatibility between I3C links @1.0V/1.8V and I2C @3.3V (e.g., I3C-compatible level shifters, muxes/switches on RunBMC, etc.) are not precluded. I3C Hubs are provided as an example how to mitigate backward compatibility problem.

Signal Name	Primary Functionality	Secondary Function	Tertiary Function
I2C1SCL_GPIO88_I3C3SCL	I2C1 Serial Clock	GPIO	I3C3 Serial Clock
I2C1SDA_ GPIO90_ I3C3SDA	I2C1 Serial Data	GPIO	I3C3 Serial Data
I2C2SCL_GPIO87_I3C4SCL	I2C2 Serial Clock	GPIO	I3C4 Serial Clock
I2C2SDA_GPIO89_ I3C4SDA	I2C2 Serial Data	GPIO	I3C4 Serial Data
I2C3SCL_GPIO119_ I3C5SCL	I2C3 Serial Clock	GPIO	I3C5 Serial Clock
I2C3SDA_GPIO121_ I3C5SDA	I2C3 Serial Data	GPIO	I3C5 Serial Data
I2C4SCL_GPIO94_ I3C6SCL	I2C4 Serial Clock	GPIO	I3C6 Serial Clock
I2C4SDA_GPIO96_ I3C6SDA	I2C4 Serial Data	GPIO	-
I2C5SCL_GPIO34	I2C5 Serial Clock	GPIO	-
I2C5SDA_GPIO36	I2C5 Serial Data	GPIO	-
I2C6SCL_GPIO30	I2C6 Serial Clock	GPIO	-
I2C6SDA_GPIO32	I2C6 Serial Data	GPIO	-
I2C7SCL_GPIO31	I2C7 Serial Clock	GPIO	-

I2C7SDA_GPIO33	I2C7 Serial Data	GPIO	-
I2C8SCL_GPIO27	I2C8 Serial Clock	GPIO	-
I2C8SDA_GPIO29	I2C8 Serial Data	GPIO	-
I2C9SCL	I2C9 Serial Clock	None	-
I2C9SDA	I2C9 Serial Data	None	-
I2C10SCL_GPIO110	I2C10 Serial Clock	GPIO	-
I2C10SDA_GPIO111	I2C10 Serial Data	GPIO	-
I2C11SCL_GPIO117	I2C11 Serial Clock	GPIO	-
I2C11SDA_GPIO118	I2C11 Serial Data	GPIO	-
I2C12SCL_GPIO100	I2C12 Serial Clock	GPIO	-
I2C12SDA_GPIO101	I2C12 Serial Data	GPIO	-
I2C13SCL_GPIO26	I2C13 Serial Clock	GPIO	-
I2C13SDA_GPIO28	I2C13 Serial Data	GPIO	-
GPIO91_I2C14SCL	GPIO	I2C14 Serial Clock	-
GPIO93_I2C14SDA	GPIO	I2C14 Serial Data	-
GPIO113_I2C15SCL_I3C2SCL	GPIO	I2C15 Serial Clock	I3C2 Serial Clock
GPIO115_I2C15SDA_I3C2SDA	GPIO	I2C15 Serial Data	I3C2 Serial Data
GPIO95_I2C16SCL_I3C1SCL	GPIO	I2C16 Serial Clock	I3C1 Serial Clock
GPIO97_I2C16SDA_I3C1SDA	GPIO	I2C16 Serial Data	I3C1 Serial Data

Table 16 I2C/I3C Busses on the RunBMC Interface

5.2.14 UART

The Interface shall provide five UARTs, but only the associated TX and RX signals are provided. Three UART interfaces are provided as primary functionality and the remaining two are available as secondary functionality. One UART shall be named CONSOLE for default BMC console output. The motherboard / system designer should take note that hardware flow control is not supported.

UART	Signal Name	Primary Functionality	Secondary Functionality
UART1	UART1RX_GPIO23	UART1 Receive Data	General Purpose Input Output
	UART1TX_GPO0	UART1 Transmit Data	General Purpose Output
UART2	UART2RX_GPIO22	UART2 Receive Data	General Purpose Input Output
	UART2TX_GPIO24	UART2 Transmit Data	General Purpose Input Output
UART3	GPIO102_UART3RX	General Purpose Input Output	UART3 Receive Data
	GPIO103_UART3TX	General Purpose Input Output	UART3 Transmit Data
UART4	GPIO104_UART4RX	General Purpose Input Output	UART4 Receive Data
	GPIO105_UART4TX	General Purpose Input Output	UART4 Transmit Data
CONSOLE (UART5)	CONSOLERX	Console UART Receive Data	None
	CONSOLETX	Console UART Transmit Data	None

Table 17 UART Signals on the RunBMC Interface

5.2.15 PWM

The Interface shall provide eight PWM (Pulse-Width Modulation) outputs. Driven from the BMC SoC these outputs are intended to drive fans or pumps present in the system. Details on frequency and other signal level specifications must be consulted from the BMC SoC Data Sheet.

The motherboard / system designer should expect that these signals will require Voltage level conversion on the Motherboard or System Board (see section 6 for the voltage levels provided over the interface). It is the responsibility of the motherboard designer to add circuitry to properly isolate the BMC signals from the fans or pumps being controlled.

Signal Name	Primary Function	Secondary Function
PWM0_GPIO10	Pulse Width Modulation Channel 0	GPIO
PWM1_GPIO12	Pulse Width Modulation Channel 1	GPIO
PWM2_GPIO9	Pulse Width Modulation Channel 2	GPIO
PWM3_GPIO14	Pulse Width Modulation Channel 3	GPIO
PWM4_GPIO11	Pulse Width Modulation Channel 4	GPIO
PWM5_GPIO16	Pulse Width Modulation Channel 5	GPIO
PWM6_GPIO13	Pulse Width Modulation Channel 6	GPIO
PWM7_GPIO18	Pulse Width Modulation Channel 7	GPIO

Table 18 Pulse Width Modulation Channels on the RunBMC Interface

5.2.16 TACH

The Interface shall provide sixteen Tachometer inputs to the BMC SoC. It is expected that these signals have the necessary level conversion before going over the interface (see section 6 for voltage levels expected). The motherboard / system designer should expect to add circuitry to properly isolate the BMC signals (those that will travel over the interface) from tachometer signals read from fans or pumps.

Signal Name	Primary Function	Secondary Function
TACH0_GPIO46	Tachometer Input 0	GPIO
TACH1_GPIO48	Tachometer Input 1	GPIO
TACH2_GPIO50	Tachometer Input 2	GPIO
TACH3_GPIO52	Tachometer Input 3	GPIO
TACH4_GPIO54	Tachometer Input 4	GPIO
TACH5_GPIO55	Tachometer Input 5	GPIO
TACH6_GPIO56	Tachometer Input 6	GPIO
TACH7_GPIO58	Tachometer Input 7	GPIO
TACH8_GPIO60	Tachometer Input 8	GPIO
TACH9_GPIO62	Tachometer Input 9	GPIO
TACH10_GPIO64	Tachometer Input 10	GPIO
TACH11_GPIO66	Tachometer Input 11	GPIO
TACH12_GPIO68	Tachometer Input 12	GPIO
TACH13_GPIO70	Tachometer Input 13	GPIO
TACH14_GPIO72	Tachometer Input 14	GPIO
TACH15_GPIO74	Tachometer Input 15	GPIO

Table 19 Tachometer Input Signals on the RunBMC Interface

5.2.17 PECI

The Interface shall provide a Platform Environment Control Interface (PECI). This Intel proprietary bus is meant to read die temperature. The interface shall provide two pins, PECI and PECIVDD. PECI is a 1-wire data signal that acts as bi-directional signal to the BMC. PECIVDD is the host voltage that defines a reference for the PECI interface. On non-Intel systems, the PECI interface may not be supported on system. When not supported, the motherboard / system designer should ensure the pins on the connector be left floating or unconnected on the system side. These signals do not support any secondary function

Signal Name	Primary Function	Secondary Function
PECI	1-wire data signal	None
PECIVDD	Host Voltage	None

Table 20 PECI Signals on the RunBMC Interface

5.2.18 PASSTHRU

The Interface shall provide 2 pairs of Pass-Through (PASSTHRU) signals that will depend upon the BMC SoC to support the Pass-Through as secondary functionality. The pair indicates an input and output signal where the signal from input will directly pass to the output, with the BMC SoC able to read the signal but not able to control it.

Signal Name	Primary Function	Secondary Function
GPIO21_PASSTHRU2_OUT	General Purpose Input Output	Pass-Through 2 output
GPIO45_PASSTHRU1_OUT	General Purpose Input Output	Pass-Through 1 output
GPIO85_PASSTHRU1_IN	General Purpose Input Output	Pass-Through 1 input
GPIO109_PASSTHRU2_IN	General Purpose Input Output	Pass-Through 2 input

Table 21 Pass-Through Signals on the RunBMC Interface

5.2.19 GPIO / GPO / GPI

The Interface shall provide a number of General Purpose signals, some of which may act as both input and output, and some which will singularly act as input or output. For the specific pins that must add this functionality see Tables 1 and 12. Any GPIO is defined in the literal sense that it may be used for the purpose of defining an input or output signal to the BMC. These are software configurable and as an example are intended for use throughout the motherboard / system as indicators, control pins, interrupts, and input logic read by the BMC. In the case of GPI and GPO, these pins are fixed as input and output respectively. Most of the interfaces described in Section 5 have GPIO, GPO, and GPI as a secondary function. There is a total of thirty-one ‘dedicated’ (that is, GPIO only) signals listed in Table 21. There are 2 signals that have new secondary function added in RunBMC 1.5 update (GPIO49, GPIO 79) and are also listed in RESET and POWERGOOD Signals.

Signal Name	Primary Function	Secondary Function
GPIO7	General Purpose Input Output	None
GPIO15	General Purpose Input Output	None
GPIO17	General Purpose Input Output	None
GPIO19	General Purpose Input Output	None
GPIO20	General Purpose Input Output	None
GPIO25	General Purpose Input Output	None
GPIO38	General Purpose Input Output	None
GPIO39	General Purpose Input Output	None
GPIO40	General Purpose Input Output	None
GPIO42	General Purpose Input Output	None
GPIO44	General Purpose Input Output	None
GPIO47	General Purpose Input Output	None
GPIO49	General Purpose Input Output	PWRGD_OUT
GPIO53	General Purpose Input Output	None
GPIO55	General Purpose Input Output	None
GPIO57	General Purpose Input Output	None
GPIO61	General Purpose Input Output	None
GPIO63	General Purpose Input Output	None
GPIO69	General Purpose Input Output	None
GPIO71	General Purpose Input Output	None
GPIO73	General Purpose Input Output	None
GPIO75	General Purpose Input Output	None

GPIO76	General Purpose Input Output	None
GPIO77	General Purpose Input Output	None
GPIO79	General Purpose Input Output	BMC_CORE_RST#
GPIO81	General Purpose Input Output	None
GPIO83	General Purpose Input Output	None
GPIO98	General Purpose Input Output	None
GPIO99	General Purpose Input Output	None
GPIO106	General Purpose Input Output	None
GPIO107	General Purpose Input Output	None
GPIO108	General Purpose Input Output	None

Table 21 Dedicated GPIO Signals on the RunBMC Interface

5.2.20 SGPIO

The Interface shall provide a single Serial GPIO interface that is capable as Master. In some modules this may also act as a slave monitor. There are four signals defined from perspective of the master in Table 22.

Signal Name	Primary Function	Secondary Function and Description
GPIO0_SGPMLD	General Purpose Input Output	Serial GPIO Serial Data Load, an output from the BMC
GPIO1_SGPMI	General Purpose Input Output	Serial GPIO Serial Data Input, an input to the BMC
GPIO3_SGPMO	General Purpose Input Output	Serial GPIO Serial Data Output, an output from the BMC
GPIO5_SGPMCK	General Purpose Input Output	Serial GPIO Clock Output, controlling clock for the bus, output from the BMC

Table 22 Serial GPIO Signals on the RunBMC Interface

5.2.21 RESETS and POWERGOOD Signals

The Interface shall provide an input, BMC_RESET# and BMC_CORE_RST# signals. Those reset signals are an active low input to the BMC SOC. BMC_RESET# shall reset the entire BMC SOC subsystem while BMC_CORE_RST# shall reset only the application cores (i.e. ARM cores or other cores running BMC FW) of the BMC subsystem. BMC_CORE_RST# is intended to be used by the Platform Root Of Trust (PROT) to hold BMC application cores in reset.

The Interface shall provide a PWRGD (Or POWERGOOD) input to the BMC. This is intended for use as a high priority interrupt and status derived from power supply status. The interface shall also provide a POWERGOOD output PWRGD_OUT indication back to baseboard form VRs on RunBMC module.

The interface shall provide a CPU_RST# input. This active low input should be used to monitor CPU resets on the host system.

Signal Name	Primary Function	Secondary Function
BMC_RESET#	Active-low BMC Subsystem Reset	None
BMC_CORE_RESET#	GPIO79	BMC Application Core(s) reset
PWRGD	Power Good indicator input to BMC	None
PWRGD_OUT	GPIO49	Power Good indicator output from RunBMC
PLT_RST#	Host CPU Platform Reset	None

Table 23 Miscellaneous Signals on the RunBMC Interface

5.2.22 WATCHDOG

The Interface shall provide two Watchdog reset output signals. These are suggested to be used to reset system components. As an example, this signal can be used to reset a TPM in the scenario of a watchdog timeout on the BMC so that the system reboots properly.

Signal Name	Primary Function	Secondary Function
WDTRST1_GPIO59	Watchdog Reset Output	GPIO
WDTRST2_GPIO51	Watchdog Reset Output	GPIO

Table 24 Watchdog Reset Outputs on the RunBMC interface

5.2.23 INDICATOR

The Interface shall provide an output called INDICATOR. This defines generic indication from the module to the system. The use of this pin is dependent on the BMC module used, so consult specific documentation for that module.

Signal Name	Primary Function	Secondary Function
GPIO37_INDICATOR#	GPIO	Active-low indicator

Table 25 Indicator Signal on RunBMC Interface

5.2.24 RESERVED

The Interface shall provide one RESERVED pin. This pin is reserved for future use or module specific functionality. Secondary function for this pin shall support GPIO.

Signal Name	Primary Function	Secondary Function
RESERVED_GPIO67	May have special functionality	GPIO

Table 26 Reserved Signal on RunBMC Interface

5.3 Pin Definition

The BMC daughter board shall have the following pinout:

Pin #	Name		Name	Pin #
1	VDD_12V_STBY		VDD_RGMII_REF	2
3	VDD3_3V_STBY		VDD3_3V_STBY	4
5	VDD3_3V_STBY		VDD3_3V_STBY	6
7	VDD3_3V_STBY		GND	8
9	GND		DACG_NC_DPTXP0	10
11	GND		DACB_NC_DPTXN0	12
13	GPIO0_SGPMLD		DACR_NC_DPHPD	14
15	GPIO1_SGPMI		VGAHS_GPIO2_DPTXP1	16
17	GPIO3_SGPMO		VGAVS_GPIO4_DPTXN1	18
19	GPIO5_SGPMCK		DDCCLK_GPIO6_DPAUXP	20
21	CONSOLERX		DDCDAT_GPIO8_DPAUXN	22
23	CONSOLETX		GND	24
25	GPIO7		PWM0_GPIO10	26
27	PWM2_GPIO9		PWM1_GPIO12	28
29	PWM4_GPIO11		PWM3_GPIO14	30
31	PWM6_GPIO13		PWM5_GPIO16	32
33	GND		PWM7_GPIO18	34
35	GPIO15		GPIO19	36

37	GPIO17		GPIO20	38
39	GND		GPIO21_PASSTHRU2_OUT	40
41	UART1RX_GPIO23		UART2RX_GPIO22	42
43	UART1TX_GPO0		UART2TX_GPIO24	44
45	GND		GPIO25	46
47	I2C8SCL_GPIO27		I2C13SCL_GPIO26	48
49	I2C8SDA_GPIO29		I2C13SDA_GPIO28	50
51	GND		GND	52
53	I2C7SCL_GPIO31		I2C6SCL_GPIO30	54
55	I2C7SDA_GPIO33		I2C6SDA_GPIO32	56
57	GND		GND	58
59	GPIO35_FWSPIWP#_SD1WP#		I2C5SCL_GPIO34	60
61	GPIO37_INDICATOR#		I2C5SDA_GPIO36	62
63	FWSPICS0#		GND	64
65	FWSPIMOSI_IO0		GPIO38	66
67	FWSPIMISO_IO1		GPIO39	68
69	FWSPI_IO2_GPIO41		GPIO40	70
71	FWSPI_IO3_GPIO43		GPIO42	72
73	FWSPICK		GPIO44	74
75	FWSPICS1#		GPIO45_PASSTHRU1_OUT	76
77	PWRGD		TACH0_GPIO46	78
79	GPIO47		TACH1_GPIO48	80
81	GPIO49_PWRGD_OUT		TACH2_GPIO50	82
83	WDTRST2_GPIO51		TACH3_GPIO52	84
85	GPIO53		TACH4_GPIO54	86
87	GPIO55		TACH5_GPIO56	88
89	GPIO57		TACH6_GPIO58	90
91	WDTRST1_GPIO59		TACH7_GPIO60	92
93	GPIO61		TACH8_GPIO62	94
95	GPIO63		TACH9_GPIO64	96
97	PLT_RST#		TACH10_GPIO65	98
99	RESERVED_GPIO67		TACH11_GPIO66	100
101	GPIO69		TACH12_GPIO68	102
103	GPIO71		TACH13_GPIO70	104
105	GPIO73		TACH14_GPIO72	106
107	GPIO75		TACH15_GPIO74	108
109	GPIO76		GND	110
111	PECIVDD		PECI	112
113	GPIO77		GND	114
115	GPIO79_BMC_CORE_RST#		SPI2CK_GPIO78	116
117	GPIO81		SPI2MISO_GPIO80	118
119	GPIO83		SPI2MOSI_GPIO82	120
121	GPIO85_PASSTHRU1_IN		SPI2CS0#_GPIO84	122
123	I2C2SCL_GPIO87_I3C4SCL		SPI2CS1#_GPIO86	124
125	I2C2SDA_GPIO89_I3C4SDA		GND	126
127	GND		I2C1SCL_GPIO88_I3C3SCL	128
129	GPIO91_I2C14SCL		I2C1SDA_GPIO90_I3C3SDA	130
131	GPIO93_I2C14SDA		GND	132
133	GND		I2C4SCL_GPIO94_I3C6SCL	134
135	GPIO95_I2C16SCL_I3C1SCL		I2C4SDA_GPIO96_I3C6SDA	136
137	GPIO97_I2C16SDA_I3C1SCL		GPIO98	138
139	GND		GPIO99	140
141	I2C12SCL_GPIO100		PERSTN	142
143	I2C12SDA_GPIO101		GPIO102_UART3RX	144
	Mechanical Key			
145	GND		GPIO103_UART3TX	146
147	PERXN		GPIO104_UART4RX	148
149	PERXP		GPIO105_UART4TX	150
151	GND		VDD_LPC3V3_ESPI1V8	152
153	PETXN		GPIO106	154
155	PETXP		GPIO107	156

157	GND		GPIO108	158
159	PEREFCLKN		GPIO109_PASSTHRU2_IN	160
161	PEREFCLKP		JTAG1TRST	162
163	GND		JTAG1TDO	164
165	LPCRST#_ESPIRST#		JTAG1TDI	166
167	LPCD1_ESPID1		JTAG1RTCK	168
169	LPCD0_ESPID0		JTAG1TCK	170
171	LPCIRQ#_ESPIALERT#		JTAG1TMS	172
173	LPCFRAME#_ESPICS#		ADC0	174
175	LPCD3_ESPID3		ADC1	176
177	LPCD2_ESPID2		ADC2	178
179	LPCCLK_ESPICLK		ADC3	180
181	I2C9SCL		ADC4	182
183	I2C9SDA		ADC5	184
185	GND		ADC6	186
187	I2C10SCL_GPIO110		ADC7	188
189	I2C10SDA_GPIO111		SYSCS#_GPIO112	190
191	GND		SYSMISO_GPO1	192
193	GPIO113_I2C15SCL_I3C2SCL		SYSMOSI_GPO2	194
195	GPIO115_I2C15SDA_I3C2SDA		SYSCK_GPIO114	196
197	GND		SPI1CS0#_GPIO116	198
199	I2C11SCL_GPIO117		SPI1MOSI_IO0_GPO3	200
201	I2C11SDA_GPIO118		SPI1MISO_IO1_GPO4	202
203	GND		GPO5_SPI1_IO2	204
205	I2C3SCL_GPIO119_I3C5SCL		GPIO120_SPI1_IO3	206
207	I2C3SDA_GPIO121_I3C5SDA		SPI1CK_GPIO122	208
209	GPIO123_USB2BVBUSSNS		SPI1CS1#_GPIO124	210
211	GPIO125_USB2AVBUSSNS		GND	212
213	GPIO126_USB2APWREN		RMIIMDIO	214
215	GND		RMIICRSDV	216
217	USB2A_HD_DN		RMIIMDC	218
219	USB2A_HD_DP		RMIIRCLKI	220
221	GND		RMIIRXER	222
223	USB2B_D_DN		RMIITXEN	224
225	USB2B_D_DP		GND	226
227	GND		RMIIRXD0	228
229	TRD0P_RGMIITXD0		RMIIRXD1	230
231	TRD0N_RGMIIRXD0		GND	232
233	GND		RMIITXD0	234
235	TRD1N_RGMIIRXD1		RMIITXD1	236
237	TRD1P_RGMIITXD1		GND	238
239	GND		PHYLED1_RGMIITXCK	240
241	TRD2P_RGMIITXD2		PHYLED2_RGMIIRXCTL	242
243	TRD2N_RGMIIRXD2		PHYLED3_RGMIITXCTL	244
245	GND		GPIO127_RGMIIMDC	246
247	TRD3N_RGMIIRXD3		GPIO128_RGMIIMDIO	248
249	TRD3P_RGMIITXD3		GPIO129_RGMIIRXCK	250
251	GND		GPI0_ADC8	252
253	BMC_RESET#		GPI1_ADC9	254
255	GPI3_ADC11		GPI2_ADC10	256
257	GPI5_ADC13		GPI4_ADC12	258
259	GPI7_ADC15		GPI6_ADC14	260

Table 27 BMC connector/edge pinout with SO-DIMM Pins

5.4 Signal Functionality and Nomenclature

The BMC pinout specification outlines the functions of the physical pins. To allow for system flexibility many of the pins in the interface must be capable of dual-function; i.e. they must provide capability for both functions.

Most of these dual function pins are achieved through multiplexing, however some pins only have a singular function. The direction column's origin is the SOC on the RunBMC module, i.e. "output" signals are driven from the SOC over the connector.

Functions	Net Name	Function 1	Function 2	Function 3	Direction	Description Function 1	Description Function 2	Description Function 3
1 GbT/RGMII/GPIO	GPIO_RGMIIRXCK	GPIO	RGMIIRXCK		BI	GPIO	RGMII 2 receive clock	
1 GbT/RGMII/GPIO	PHYLED1_RGMIITXCK	PHYLED1	RGMIITXCK		BI	GPIO intended for MAGJACK LEDs, or signal from PHY	RGMII 2 transmit clock	
1 GbT/RGMII/GPIO	PHYLED2_RGMIIRXCTL	PHYLED2	RGMIIRXCTL		BI	GPIO intended for MAGJACK LEDs, or signal from PHY	RGMII 2 receive control	
1 GbT/RGMII/GPIO	PHYLED3_RGMIITXCTL	PHYLED3	RGMIITXCTL		BI	GPIO intended for MAGJACK LEDs, or signal from PHY	RGMII 2 transmit control	
1 GbT/RGMII/GPIO	GPIO_RGMIIMDC	GPIO	RGMIIMDC		OUTPUT	GPIO	Management Data Clock. The MDC clock input must be provided to allow MII management functions.	
1 GbT/RGMII/GPIO	GPIO_RGMIIMDIO	GPIO	RGMIIMDIO		BI	GPIO	Management Data I/O. This serial input/output bit is used to read from and write to the MII registers	
1 GbT/RGMII/GPIO	TRD0N_RGMIIRXD0	TRD0N	RGMIIRXD0		BI	Transmit/Receive Pair 0	RGMII 2 receive data bus from PHY bit 0	
1 GbT/RGMII/GPIO	TRD0P_RGMIITXD0	TRD0P	RGMIITXD0		BI	Transmit/Receive Pair 0	RGMII 2 transmit data bus to PHY bit 0	
1 GbT/RGMII/GPIO	TRD1N_RGMIIRXD1	TRD1N	RGMIIRXD1		BI	Transmit/Receive Pair 1	RGMII 2 receive data bus from PHY bit 1	
1 GbT/RGMII/GPIO	TRD1P_RGMIITXD1	TRD1P	RGMIITXD1		BI	Transmit/Receive Pair 1	RGMII 2 transmit data bus to PHY bit 1	
1 GbT/RGMII/GPIO	TRD2N_RGMIIRXD2	TRD2N	RGMIIRXD2		BI	Transmit/Receive Pair 2	RGMII 2 receive data bus from PHY bit 2	
1 GbT/RGMII/GPIO	TRD2P_RGMIITXD2	TRD2P	RGMIITXD2		BI	Transmit/Receive Pair 2	RGMII 2 transmit data bus to PHY bit 2	
1 GbT/RGMII/GPIO	TRD3N_RGMIIRXD3	TRD3N	RGMIIRXD3		BI	Transmit/Receive Pair 3	RGMII 2 receive data bus from PHY bit 3	
1 GbT/RGMII/GPIO	TRD3P_RGMIITXD3	TRD3P	RGMIITXD3		BI	Transmit/Receive Pair 3	RGMII 2 transmit data bus to PHY bit 3	
1.8V or 3.3V	VDD_RGMII_REF	VDD_RGMII_REF			Output	Reference voltage output for PCB RGMII PHY	none	
12v	VDD_12V_STBY	VDD_12V_STBY			Power	12v supply to PCB	none	
3.3V	VDD3_3V_STBY	VDD3_3V_STBY			Power	3.3v supply to PCB	none	
3.3V	VDD3_3V_STBY	VDD3_3V_STBY			Power	3.3v supply to PCB	none	
3.3V	VDD3_3V_STBY	VDD3_3V_STBY			Power	3.3v supply to PCB	none	
3.3V	VDD3_3V_STBY	VDD3_3V_STBY			Power	3.3v supply to PCB	none	
3.3V	VDD3_3V_STBY	VDD3_3V_STBY			Power	3.3v supply to PCB	none	
3.3Vlpc or 1.8espi	VDD_LPC3V3_ESPI1V8	VDD_LPC3V3	ESPI1V8		Input	3.3v supply to PCB LPC/eSPI	1.8v supply if needed for eSPI	
ADC	ADC0	ADC0			INPUT	channel 0 analog input		
ADC	ADC1	ADC1			INPUT	channel 1 analog input		
ADC	ADC2	ADC2			INPUT	channel 2 analog input		
ADC	ADC3	ADC3			INPUT	channel 3 analog input		
ADC	ADC4	ADC4			INPUT	channel 4 analog input		
ADC	ADC5	ADC5			INPUT	channel 5 analog input		
ADC	ADC6	ADC6			INPUT	channel 6 analog input		

Functions	Net Name	Function 1	Function 2	Function 3	Direction	Description Function 1	Description Function 2	Description Function 3
ADC	ADC7	ADC7			INPUT	channel 7 analog input		
ADC/GPIO	GPI_ADC10	GPI	ADC10		INPUT	GPI	channel 10 analog input	
ADC/GPIO	GPI_ADC11	GPI	ADC11		INPUT	GPI	channel 11 analog input	
ADC/GPIO	GPI_ADC12	GPI	ADC12		INPUT	GPI	channel 12 analog input	
ADC/GPIO	GPI_ADC13	GPI	ADC13		INPUT	GPI	channel 13 analog input	
ADC/GPIO	GPI_ADC14	GPI	ADC14		INPUT	GPI	channel 14 analog input	
ADC/GPIO	GPI_ADC15	GPI	ADC15		INPUT	GPI	channel 15 analog input	
ADC/GPIO	GPI_ADC8	GPI	ADC8		INPUT	GPI	channel 8 analog input	
ADC/GPIO	GPI_ADC9	GPI	ADC9		INPUT	GPI	channel 9 analog input	
FWSPI	FWSPICK	FWSPICK			OUTPUT	BMC FW clock output for FW living on MB		
FWSPI	FWSPICS0#	FWSPICS0#			OUTPUT	BMC FW chip select 0 for FW living on MB		
FWSPI	FWSPICS1#	FWSPICS1#			OUTPUT	BMC FW chip select 1 for FW living on MB		
FWSPI	FWSPIMISO_IO1	FWSPIMISO_IO1			BI	BMC FW MISO/IO0 for FW living on MB		
FWSPI	FWSPIMOSI_IO0	FWSPIMOSI_IO0			BI	BMC FW MOSI/IO1 for FW living on MB		
FWSPI	FWSPI_IO2_GPIO	FWSPI_IO2	GPIO		BI	BMC FW IO2 for FW living on MB to support quad	GPIO	
FWSPI	FWSPI_IO3_GPIO	FWSPI_IO3	GPIO		BI	BMC FW IO3 for FW living on MB to support quad	GPIO	
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		

Functions	Net Name	Function 1	Function 2	Function 3	Direction	Description Function 1	Description Function 2	Description Function 3
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GND	GND	GND				GND		
GPIO	GPIO	GPIO			BI	GPIO		
GPIO	GPIO	GPIO			BI	GPIO		
GPIO	GPIO	GPIO			BI	GPIO		
GPIO	GPIO	GPIO			BI	GPIO		
GPIO	GPIO	GPIO			BI	GPIO		
GPIO	GPIO	GPIO			BI	GPIO		
GPIO	GPIO	GPIO			BI	GPIO		
GPIO	GPIO	GPIO			BI	GPIO		
GPIO	GPIO	GPIO			BI	GPIO		
GPIO	GPIO	GPIO			BI	GPIO		
GPIO	GPIO	GPIO			BI	GPIO		
GPIO	GPIO	GPIO			BI	GPIO		
GPIO	GPIO	GPIO			BI	GPIO		
GPIO	GPIO	GPIO			BI	GPIO		
GPIO	GPIO	GPIO			BI	GPIO		
GPIO	GPIO	GPIO			BI	GPIO		
GPIO	GPIO	GPIO			BI	GPIO		
GPIO	GPIO	GPIO			BI	GPIO		
GPIO	GPIO	GPIO			BI	GPIO		
GPIO	GPIO	GPIO			BI	GPIO		
GPIO	GPIO	GPIO			BI	GPIO		
GPIO	GPIO	GPIO			BI	GPIO		
GPIO	GPIO	GPIO			BI	GPIO		
GPIO	GPIO	GPIO			BI	GPIO		

Functions	Net Name	Function 1	Function 2	Function 3	Direction	Description Function 1	Description Function 2	Description Function 3
GPIO	GPIO	GPIO			BI	GPIO		
GPIO	GPIO	GPIO			BI	GPIO		
GPIO	GPIO	GPIO			BI	GPIO		
GPIO	GPIO	GPIO			BI	GPIO		
GPIO	GPIO	GPIO			BI	GPIO		
GPIO/PASSTHRU	GPIO_PASSTHRU1_IN	GPIO	PASSTHRU1_IN		BI	GPIO	PASS-THROUGH 1 Input	
GPIO/PASSTHRU	GPIO_PASSTHRU1_OUT	GPIO	PASSTHRU1_OUT		BI	GPIO	PASS-THROUGH 1 Output	
GPIO/PASSTHRU	GPIO_PASSTHRU2_IN	GPIO	PASSTHRU2_IN		BI	GPIO	PASS-THROUGH 2 Input	
GPIO/PASSTHRU	GPIO_PASSTHRU2_OUT	GPIO	PASSTHRU2_OUT		BI	GPIO	PASS-THROUGH 2 Output	
I2C	I2C10SCL_GPIO	I2C10SCL	GPIO		BI	I2C/SMBUS 10 clock	GPIO	
I2C	I2C10SDA_GPIO	I2C10SDA	GPIO		BI	I2C/SMBUS 10 data	GPIO	
I2C	I2C11SCL_GPIO	I2C11SCL	GPIO		BI	I2C/SMBUS 11 clock	GPIO	
I2C	I2C11SDA_GPIO	I2C11SDA	GPIO		BI	I2C/SMBUS 11 data	GPIO	
I2C	I2C12SCL_GPIO	I2C12SCL	GPIO		BI	I2C/SMBUS 12 clock	GPIO	
I2C	I2C12SDA_GPIO	I2C12SDA	GPIO		BI	I2C/SMBUS 12 data	GPIO	
I2C	I2C1SCL_GPIO_I3C3SCL	I2C1SCL	GPIO	I3C3SCL	BI	I2C/SMBUS 1 clock	GPIO	I3C3 Serial Clock
I2C	I2C1SDA_GPIO_I3C3SDA	I2C1SDA	GPIO	I3C3SDA	BI	I2C/SMBUS 1 data	GPIO	I3C3 Serial Data
I2C	I2C2SCL_GPIO_I3C4SCL	I2C2SCL	GPIO	I3C4SCL	BI	I2C/SMBUS 2 clock	GPIO	I3C4 Serial Clock
I2C	I2C2SDA_GPIO_I3C4SDA	I2C2SDA	GPIO	I3C4SDA	BI	I2C/SMBUS 2 data	GPIO	I3C4 Serial Data
I2C	I2C3SCL_GPIO_I3C5SCL	I2C3SCL	GPIO	I3C5SCL	BI	I2C/SMBUS 3 clock	GPIO	I3C5 Serial Clock
I2C	I2C3SDA_GPIO_I3C5SDA	I2C3SDA	GPIO	I3C5SDA	BI	I2C/SMBUS 3 data	GPIO	I3C5 Serial Data
I2C	I2C4SCL_GPIO_I3C6SCL	I2C4SCL	GPIO	I3C6SCL	BI	I2C/SMBUS 4 clock	GPIO	I3C6 Serial Clock
I2C	I2C4SDA_GPIO_I3C6SDA	I2C4SDA	GPIO	I3C6SDA	BI	I2C/SMBUS 4 data	GPIO	I3C3 Serial Clock
I2C	I2C5SCL_GPIO	I2C5SCL	GPIO		BI	I2C/SMBUS 5 clock	GPIO	
I2C	I2C5SDA_GPIO	I2C5SDA	GPIO		BI	I2C/SMBUS 5 data	GPIO	
I2C	I2C6SCL_GPIO	I2C6SCL	GPIO		BI	I2C/SMBUS 6 clock	GPIO	
I2C	I2C6SDA_GPIO	I2C6SDA	GPIO		BI	I2C/SMBUS 6 data	GPIO	
I2C	I2C7SCL_GPIO	I2C7SCL	GPIO		BI	I2C/SMBUS 7 clock	GPIO	
I2C	I2C7SDA_GPIO	I2C7SDA	GPIO		BI	I2C/SMBUS 7 data	GPIO	
I2C	I2C8SCL_GPIO	I2C8SCL	GPIO		BI	I2C/SMBUS 8 clock	GPIO	
I2C	I2C8SDA_GPIO	I2C8SDA	GPIO		BI	I2C/SMBUS 8 data	GPIO	
I2C	I2C9SCL	I2C9SCL			BI	I2C/SMBUS 9 clock	GPIO	
I2C	I2C9SDA	I2C9SDA			BI	I2C/SMBUS 9 data	GPIO	
I2C	I2C13SCL_GPIO	I2C13SCL	GPIO		BI	I2C/SMBUS 13 clock	GPIO	
I2C	I2C13SDA_GPIO	I2C13SDA	GPIO		BI	I2C/SMBUS 13 data	GPIO	
I2C	GPIO_I2C14SCL	GPIO	I2C14SCL		BI	GPIO	I2C/SMBUS 14 clock	
I2C	GPIO_I2C14SDA	GPIO	I2C14SDA		BI	GPIO	I2C/SMBUS 14 data	
I2C	GPIO_I2C15SCL	GPIO	I2C15SCL	I3C2SCL	BI	GPIO	I2C/SMBUS 15 clock	I3C2 Serial Clock
I2C	GPIO_I2C15SDA	GPIO	I2C15SDA	I3C2SDA	BI	GPIO	I2C/SMBUS 15 data	I3C2 Serial Data

Functions	Net Name	Function 1	Function 2	Function 3	Direction	Description Function 1	Description Function 2	Description Function 3
I2C	GPIO_I2C16SCL	GPIO	I2C16SCL	I3C1SCL	BI	GPIO	I2C/SMBUS 16 clock	I3C1 Serial Clock
I2C	GPIO_I2C16SDA	GPIO	I2C16SDA	I3C1SDA	BI	GPIO	I2C/SMBUS 16 data	I3C1 Serial Data
INDICATOR	GPIO_INDICATOR	GPIO	INDICATOR		BI	Boot indication from BMC / GPIO option	GPIO	
JTAG	JTAG1RTCK	JTAG1RTCK			INPUT	JTAG Return Test Clock Input		
JTAG	JTAG1TCK	JTAG1TCK			OUTPUT	JTAG Master Clock Output		
JTAG	JTAG1TDI	JTAG1TDI			OUTPUT	JTAG Master Data Output		
JTAG	JTAG1TDO	JTAG1TDO			INPUT	JTAG Master Data Input		
JTAG	JTAG1TMS	JTAG1TMS			OUTPUT	JTAG Master Mode Select Output		
JTAG	JTAG1TRST	JTAG1TRST			OUTPUT	JTAG Test Reset Output		
LPC/eSPI	LPCCLK_ESPICLK	LPCCLK	ESPICLK		INPUT	LPC bus clock input (default)	eSPI clock input	
LPC/eSPI	LPCD0_ESPID0	LPCD0	ESPID0		BI	LPC address and data bus bit 0	eSPI data bus bit 0	
LPC/eSPI	LPCD1_ESPID1	LPCD1	ESPID1		BI	LPC address and data bus bit 1	eSPI data bus bit 1	
LPC/eSPI	LPCD2_ESPID2	LPCD2	ESPID2		BI	LPC address and data bus bit 2	eSPI data bus bit 2	
LPC/eSPI	LPCD3_ESPID3	LPCD3	ESPID3		BI	LPC address and data bus bit 3	eSPI data bus bit 3	
LPC/eSPI	LPCFRAME#_ESPICS#	LPCFRAME#	ESPICS#		INPUT	LPC FRAME# (default)	eSPI chip select input	
LPC/eSPI	LPCIRQ#_ESPIALERT#	LPCIRQ#	ESPIALERT#		BI	LPC serial IRQ (default)	eSPI Alert	
LPC/eSPI	LPCRST#_ESPIRST#	LPCRST#	ESPIRST#		INPUT	LPC reset input (default)	eSPI reset input	
PCIE	PEREFCLKN	PEREFCLKN			INPUT	PCI Express Reference clock input, 100MHz negative input of the differential clock pair	none	
PCIE	PEREFCLKP	PEREFCLKP			INPUT	PCI Express Reference clock input, 100MHz positive input of the differential clock pair	none	
PCIE	PERSTN	PERSTN			OUTPUT	PCI Express reset pin This reset signal reset PCI Express bus controller and VGA/2D device.	none	
PCIE	PERXN	PERXN			INPUT	PCI Express Serial Data Receiver It receives negative input of the differential signal pair.	none	
PCIE	PERXP	PERXP			INPUT	PCI Express Serial Data Receiver It receives positive input of the differential signal pair.	none	
PCIE	PETXN	PETXN			OUTPUT	PCI Express Serial Data Transmitter It transmits negative output of the differential signal pa	none	
PCIE	PETXP	PETXP			OUTPUT	PCI Express Serial Data Transmitter It transmits positive output of the differential signal pair.	none	
PECI	PECI	PECI			INPUT	PECI signal input/output to BMC	none	
PECI	PECIVDD	PECIVDD			INPUT	PECI power	none	
PWM/GPIO	PWM0_GPIO	PWM0	GPIO		BI	PWM output	GPIO	
PWM/GPIO	PWM1_GPIO	PWM1	GPIO		BI	PWM output	GPIO	
PWM/GPIO	PWM2_GPIO	PWM2	GPIO		BI	PWM output	GPIO	

Functions	Net Name	Function 1	Function 2	Function 3	Direction	Description Function 1	Description Function 2	Description Function 3
PWM/GPIO	PWM3_GPIO	PWM3	GPIO		BI	PWM output	GPIO	
PWM/GPIO	PWM4_GPIO	PWM4	GPIO		BI	PWM output	GPIO	
PWM/GPIO	PWM5_GPIO	PWM5	GPIO		BI	PWM output	GPIO	
PWM/GPIO	PWM6_GPIO	PWM6	GPIO		BI	PWM output	GPIO	
PWM/GPIO	PWM7_GPIO	PWM7	GPIO		BI	PWM output	GPIO	
RESET	BMC_RESET#	BMC_RESET#			INPUT	Core Reset circuitry for SOC and any periphery components needed for reset		
RESET	GPIO_BMC_CORE_RESET#	GPIO	BMC_CORE_RESET#		BI	BMC Application Core(s) reset		
RESET	PWRGD	PWRGD			INPUT	power Good from power supply		
RESET	GPIO_PWRGD_OUT	GPIO	PWRGD_OUT		BI	Power Good indicator output from RunBMC		
RFU	RESERVED_GPIO	RESERVED	GPIO		BI	Can Be Reserved for module specific use	GPIO	
RESET	PLT_RST#	PLT_RST#			INPUT	Host CPU PlatformReset		
RMII	RMIICRSDV	RMIICRSDV			INPUT	RMII/NCSI 1 receive carrier sense and data valid		
RMII	RMIIMDC	RMIIMDC			OUTPUT	Management Data Clock. The MDC clock input must be provided to allow MII management functions.		
RMII	RMIIMDIO	RMIIMDIO			BI	Management Data I/O. This serial input/output bit is used to read from and write to the MII registers		
RMII	RMIIRCLKI	RMIIRCLKI			INPUT	RMII/NCSI 1 50MHz reference clock input		
RMII	RMIIRXD0	RMIIRXD0			INPUT	RMII/NCSI 1 receive data bus from PHY bit 0		
RMII	RMIIRXD1	RMIIRXD1			INPUT	RMII/NCSI 1 receive data bus from PHY bit 1		
RMII	RMIIRXER	RMIIRXER			INPUT	RMII/NCSI 1 receive data error		
RMII	RMIITXD0	RMIITXD0			OUTPUT	RMII/NCSI 1 transmit data bus to PHY bit 0		
RMII	RMIITXD1	RMIITXD1			OUTPUT	RMII/NCSI 1 transmit data bus to PHY bit 1		
RMII	RMIITXEN	RMIITXEN			OUTPUT	RMII/NCSI 1 transmit enable		
SGPIO/GPIO	GPIO_SGPMCK	GPIO	SGPMCK		OUTPUT	GPIO	Master Serial GPIO clock output	
SGPIO/GPIO	GPIO_SGPMI	GPIO	SGPMI		INPUT	GPIO	Master Serial GPIO serial data input	
SGPIO/GPIO	GPIO_SGPMLD	GPIO	SGPMLD		OUTPUT	GPIO	Master Serial GPIO serial data load output	
SGPIO/GPIO	GPIO_SGPMO	GPIO	SGPMO		OUTPUT	GPIO	Master Serial GPIO serial data output	
SPI/GPIO	SPI1MISO_IO1_GPO	SPI1MISO_IO1	GPO		BI	SPI 1 MISO/IO1	GPO	
SPI/GPIO	SPI1MOSI_IO0_GPO	SPI1MOSI_IO0	GPO		BI	SPI 1 MOSI/IO0	GPO	
SPI/GPIO	SPI1CK_GPIO	SPI1CK	GPIO		BI	SPI 1 clock output	GPIO	
SPI/GPIO	SPI1CS0#_GPIO	SPI1CS0#	GPIO		BI	SPI 1 chip select 0	GPIO	
SPI/GPIO	SPI1CS1#_GPIO	SPI1CS1#	GPIO		BI	SPI 1 chip select 1	GPIO	
SPI/GPIO	GPO_SPI1_IO2	GPO	SPI1_IO2		BI	GPO	SPI1 IO2 to support quad	
SPI/GPIO	GPIO_SPI1_IO3	GPIO	SPI1_IO3		BI	GPIO	SPI1 IO3 to support quad	
SPI/GPIO	SPI2CK_GPIO	SPI2CK	GPIO		BI	SPI 2 clock output	GPIO	
SPI/GPIO	SPI2CS0#_GPIO	SPI2CS0#	GPIO		BI	SPI 2 chip select 0	GPIO	

Functions	Net Name	Function 1	Function 2	Function 3	Direction	Description Function 1	Description Function 2	Description Function 3
SPI/GPIO	SPI2CS1#_GPIO	SPI2CS1#	GPIO		BI	SPI 2 chip select 1	GPIO	
SPI/GPIO	SPI2MISO_GPIO	SPI2MISO	GPIO		BI	SPI 2 MISO	GPIO	
SPI/GPIO	SPI2MOSI_GPIO	SPI2MOSI	GPIO		BI	SPI 2 MOSI	GPIO	
SPI/GPIO	SYSCS#_GPIO	SYSCS#	GPIO		BI	System SPI Chip Select input	GPIO	
SPI/GPIO	SYSMISO_GPO	SYSMISO	GPO		BI	System SPI MOSI	GPO	
SPI/GPIO	SYSMOSI_GPO	SYSMOSI	GPO		OUTPUT	System SPI MISO	GPO	
SPI/GPIO	SYSCK_GPIO	SYSCK	GPIO		BI	System SPI Clock input	GPIO	
TACH/GPIO	TACH0_GPIO	TACH0	GPIO		BI	Fan Tachometer input	GPIO	
TACH/GPIO	TACH1_GPIO	TACH1	GPIO		BI	Fan Tachometer input	GPIO	
TACH/GPIO	TACH10_GPIO	TACH10	GPIO		BI	Fan Tachometer input	GPIO	
TACH/GPIO	TACH11_GPIO	TACH11	GPIO		BI	Fan Tachometer input	GPIO	
TACH/GPIO	TACH12_GPIO	TACH12	GPIO		BI	Fan Tachometer input	GPIO	
TACH/GPIO	TACH13_GPIO	TACH13	GPIO		BI	Fan Tachometer input	GPIO	
TACH/GPIO	TACH14_GPIO	TACH14	GPIO		BI	Fan Tachometer input	GPIO	
TACH/GPIO	TACH15_GPIO	TACH15	GPIO		BI	Fan Tachometer input	GPIO	
TACH/GPIO	TACH2_GPIO	TACH2	GPIO		BI	Fan Tachometer input	GPIO	
TACH/GPIO	TACH3_GPIO	TACH3	GPIO		BI	Fan Tachometer input	GPIO	
TACH/GPIO	TACH4_GPIO	TACH4	GPIO		BI	Fan Tachometer input	GPIO	
TACH/GPIO	TACH5_GPIO	TACH5	GPIO		BI	Fan Tachometer input	GPIO	
TACH/GPIO	TACH6_GPIO	TACH6	GPIO		BI	Fan Tachometer input	GPIO	
TACH/GPIO	TACH7_GPIO	TACH7	GPIO		BI	Fan Tachometer input	GPIO	
TACH/GPIO	TACH8_GPIO	TACH8	GPIO		BI	Fan Tachometer input	GPIO	
TACH/GPIO	TACH9_GPIO	TACH9	GPIO		BI	Fan Tachometer input	GPIO	
UART	CONSOLETX_GPIO	CONSOLETX	GPIO		BI	Transmit serial data output, primary console		
UART	CONSOLERX_GPIO	CONSOLERX	GPIO		BI	Receive serial data input, primary console		
UART	UART1TX_GPIO	UART1TX	GPIO		BI	Transmit serial data output		
UART	UART1RX_GPIO	UART1RX	GPIO		BI	Receive serial data input		
UART	UART2TX_GPIO	UART2TX	GPIO		BI	Transmit serial data output		
UART	UART2RX_GPIO	UART2RX	GPIO		BI	Receive serial data input		
UART	GPIO_UART3TX	GPIO	UART3TX		BI	Transmit serial data output		
UART	GPIO_UART3RX	GPIO	UART3RX		BI	Receive serial data input		
UART	GPIO_UART4TX	GPIO	UART4TX		BI	Transmit serial data output		
UART	GPIO_UART4RX	GPIO	UART4RX		BI	Receive serial data input		
USB	USB2A_HD_DN	USB2A_HD_DN			BI	Host/Device D− signal of USB 2.0 port A, USB host		
USB	USB2A_HD_DP	USB2A_HD_DP			BI	Host/Device D+ signal of USB 2.0 port A, USB host		
USB	GPIO_USB2AVBUSOVC	GPIO	USB2AVBUSOVC		BI	Host/Device Overcurrent sense	GPIO	
USB	GPIO_USB2AVBUSC	GPIO	USB2AVBUSC		BI	Host/Device VBUS Control	GPIO	
USB	USB2B_D_DN	USB2B_D_DN			BI	Device D− signal of USB 2.0 port B, device		

Functions	Net Name	Function 1	Function 2	Function 3	Direction	Description Function 1	Description Function 2	Description Function 3
USB	USB2B_D_DP	USB2B_D_DP			BI	Device D+ signal of USB 2.0 port B, device		
USB	GPIO_USB2BVBUSSNS	GPIO	USB2BVBUSSNS		BI	Device VBUS Sense	GPIO	
VGA	DACB	DACB		DPTX0	OUTPUT	DAC B channel output	Not connected	Display Port Lane 0 (+)
VGA	DACG	DACG		DPTXN0	OUTPUT	DAC G channel output	Not connected	Display Port Lane 0 (-)
VGA	DACR	DACR		DPHPD	OUTPUT	DAC R channel output	Not connected	Display Port Hot Plug Detect
VGA	DDCCLK_GPIO	DDCCLK	GPIO	DPTXP1	BI	VGA DDC clock pin	GPIO	Display Port Lane 1 (+)
VGA	DDCDAT_GPIO	DDCDAT	GPIO	DPTXN1	BI	VGA DDC data pin	GPIO	Display Port Lane 1 (-)
VGA	VGAHS_GPIO	VGAHS	GPIO	DPAUXP	BI	VGA horizontal sync output	GPIO	Display Port Aux Channel (+)
VGA	VGAVS_GPIO	VGAVS	GPIO	DPAUXN	BI	VGA vertical sync output	GPIO	Display Port Lane 0 (-)
WATCHDOG/GPIO	WDTRST1_GPIO	WDTRST1	GPIO		OUTPUT	Watchdog timer 1 pulse output	GPIO	
WATCHDOG/GPIO	WDTRST2_GPIO	WDTRST2	GPIO		OUTPUT	Watchdog timer 2 pulse output	GPIO	

Table 28 BMC Pin Functions describing both Function 1 and Function 2

6. Electrical and Timing Requirements

6.1 Electrical Requirements

DC Electrical Requirements	Requirement	Notes
Current carrying capability at 30 °C temperature rise per contact	0.50 amp/pin De-rated	Electrical Requirements shall meet PS-003A-01 JEDEC specification

Table 29 Current per pin

Power / Ground Rail	Pin Count	Description	Maximum Current/Power
VDD_12V_STBY	1	+12V main or +12V aux	0.5amps/6watts
VDD3_3V_STBY	5	+3.3V main or +3.3V aux	2.5amps/8.25watts
GND	38	Ground Return	

Table 30 Power for different Power Rails

Signal Subsystem	Description	Notes	Typical
I2C	I2C serial data (SDA) and serial clock (SCL) signals.	Pullups should be placed on System Board.	3.3V (TTL or CMOS)
I3C	I3C serial data (SDA) and serial clock (SCL) signals.	Pullups are not required. If used, then pullups should be placed on System Board.	1.0V or 1.8V
RGB	Video Graphics Array RGB signals	Filtering should be as described in Figure 5-1	0.7V (peak to peak)
TACH	Fan Tachometer Controller	Tachometer Input	3.3V (TTL or CMOS)
PWM	Pulse Width Modulation	Output	3.3V, 8mA drive strength
RGMII	Reduced Gigabit Media Independent Interface	If lower voltages are desired (ex: 1.8v), the RunBMC daughterboard must translate to 3.3V. VDD_RGMII_REF can be used as a reference voltage to translate.	3.3V or 1.8V, i.e. VDD_RGMII_REF
ADC	Analog to Digital Converter	Inputs are reference to 1.8V (ADC0-15)	1.8V (peak to peak from reference)
ESPI or LPC	Enhanced Serial Peripheral Interface Bus or Low Pin Count Interface	Voltage is selectable by VDD_LPC3V3_ESPI1V8 voltage pin.	3.3V or 1.8V (TTL or CMOS)
VDD_RGMII_REF	Voltage reference output	For scenarios where BMC's have different RGMII voltage IO requirements. This signal can be referenced on the MB for 1v8 or 3v3 I/O references. See figure 6.1 for an example.	Up to designer.

Table 31 Voltage signal requirements by Subsystem

6.1.1 VDD_RGMII_REF Signal Usage

Figure 6-1 is an example of VDD_RGMII_REF driving a voltage reference pin in the case where the BMC vendor has specific RGMII voltage requirements. For example, 1.8V HSTL vs 3.3V TTL. Usage of this signal is optional and meant to provide convenience for the motherboard / system designer. The RunBMC Module designer should have specific notes in module specific documentation on what voltage to expect on this signal.

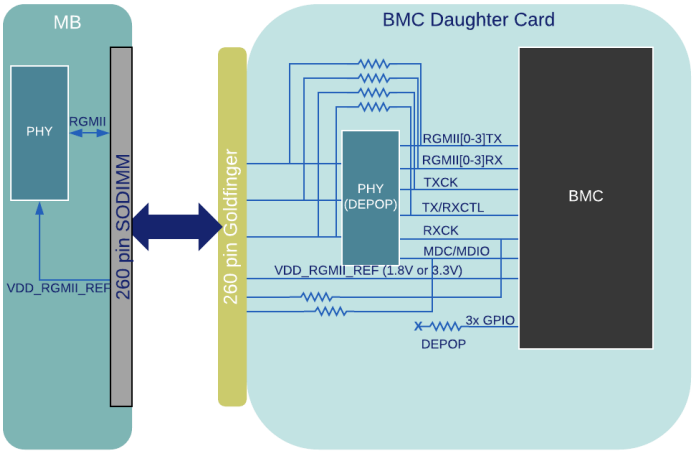


Figure 6-1 RGMII Reference Voltage for Off-Board PHY

6.2 Timing Requirements

The general recommendations for motherboard designer to consider are listed in the Table 32. Module designers should reference this section as well to understand expected skew.

Skew Requirements	Requirement	Notes
PCIe	Trace length < 17". Intra pair skew less than 3mil	Condition based on middle loss material for PCB design
USB	Trace length < 17". Intra pair skew less than 2mil	Condition based on middle loss material for PCB design
1GbT	Intra pair skew less than 2mil	Length follow PHY controller requirement with 0.5" length reduction.
RGMII	Group signal (TX and RX) skew less than 50mil	
VGA	Group signal (TX and RX) skew less than 30mil	
RMII/NC-SI	Group signal (TX and RX) skew less than 200mil	
LPC	Group signal skew less than 250mil	
SPI	Group signal (TX and RX) skew less than 100mil	

Table 32 Skew Requirements

7. Mechanical

7.1 Form Factor

The BMC module shall conform to the 260 Pin DDR4 SODIMM, .50mm Pitch DIMM Registration form factor, defined by MO-310C, with the exception of the height, component height keepout, and width requirements. The module has a 260 pin edge connector. Refer to JEDEC spec for dimensions and tolerances.

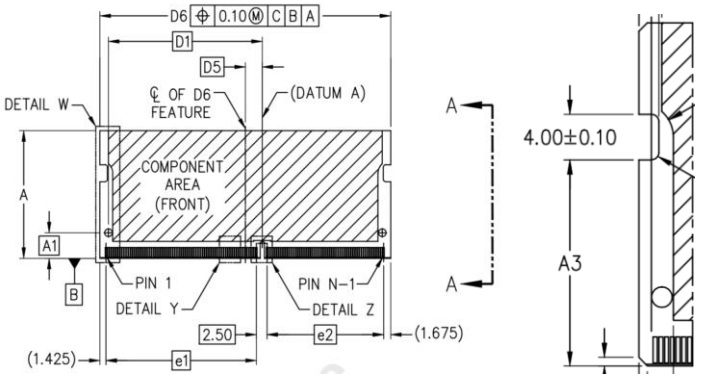


Figure 7-1 SO-DIMM Dimensions

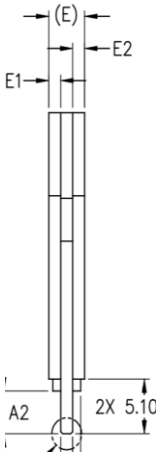
Figure 7-1 outlines the SO-DIMM DDR4 JEDEC registration. RunBMC shall follow this registration, with the exceptions to the “A” height and “D6” width. The Table 33 shows the permissible A heights and D6 widths.

Card Types	“A” height denoted in Figure 7-1	“D6” width denoted in Figure 7-1
Standard	32mm	No requirement
Large	50mm	No requirement
X-Large	70mm	No Requirement

Table 33 Dimensions for various Card Types

7.2 Component Height Keep-out Requirements

RunBMC modules shall have major components on the top side of the PCB with component height to not exceed dimension E1 in Figure 7-3. Smaller components with low height may be placed on the bottom, E2. When placed in a right-angle configuration, E1 will face towards the top (lid) of the compute or network platform.



Dimension for Figure 7-3	Size	Notes
E1 (top)	5.44mm	Right Angle config. This is the top of the PCB
PCB thickness	1.2mm	PCB material thickness
E2 (bottom)	1.6mm	Right Angle config. This is the bottom of the PCB

Figure 7-3 (left) detailing component height & Table 34 Dimensions for component height

As a recommendation for physical layout, and a note to the motherboard / system designer, the dimensions specified should allow the RunBMC module to fit in underneath a Low-Profile

PCIe card. Figure 7-4 demonstrates a right angle SO-DIMM connector of ~8mm height, with listed safety gaps and other component heights. The module placement can then be left to the MB designer with considerations for thermals (See section 8) and local component heights as shown. This Figure makes no guarantees about conformance of a right angle SO-DIMM connector (See section 7.4).

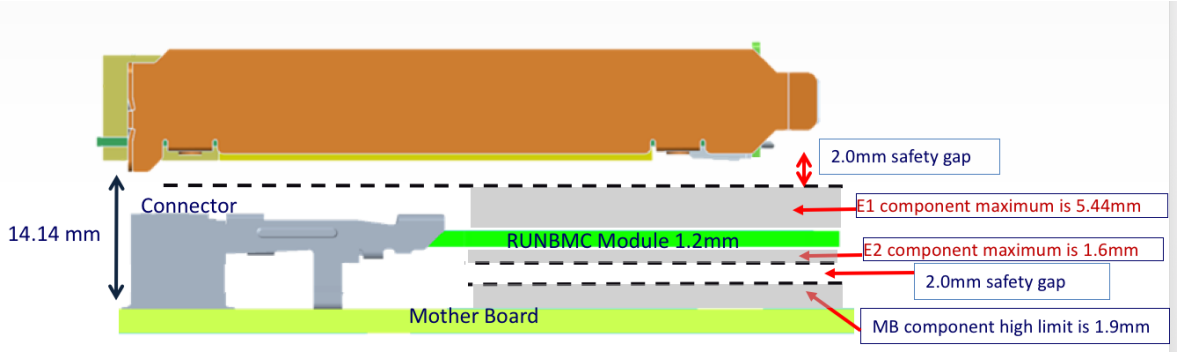


Figure 7-2 RunBMC Module shown under PCIe Bracket

7.3 RU/OU Mounting Options

In systems that are meant to fit into a standard 1 RU or 1 OU chassis, the standard size module shall support being vertically mounted. In those same systems both the standard size module and the large sized module shall support right-angle mounting.

In systems that fit into a chassis which is greater than 1 RU or 1 OU, any size of module (both standard and large) shall support both right-angle and vertical mounting.

7.4 Mating Connector

The BMC mating connector shall conform to the DDR4 Small Outline Dual Inline Memory Module (SODIMM), 260 pin, 0.50 mm pitch Socket Outline, defined by SO-018D.

A conforming vertical connector, Amphenol G634B2610X22HR, or equivalent can be mounted on the motherboard or network device, to mate with the BMC module edge connector. Right Angle or Angled connectors are permissible if conformant to SO-18D specification.

8. Thermal

The BMC mezzanine card can be located in any position of the server or network motherboard. The worst-case environmental conditions should be simulated by system designer. The thermal solution, component selections, and system design should consider for these conditions. The boundary conditions are found in Table 35 & 36.

Condition	Low	Typical	High	Max
Hot Aisle Air Temperature Boundary Conditions for Local Inlet Air Temperature	5°C (system Inlet)	55°C	60°C	65°C
Hot Aisle Airflow Boundary Conditions for Local Inlet Air Velocity	100LFM	200LFM	350LFM	System Dependent

Table 35 Thermal Boundary Conditions Assuming Hot Aisle Containment

Condition	Low	Typical	High	Max
Cold Aisle Air Temperature Boundary Conditions for Local Inlet Air Temperature	5°C	25°-35°C ASHRAE A1/A2	40°C ASHRAE A3	45°C ASHRAE A4
Cold Aisle Airflow Boundary Conditions Local Inlet Air Velocity	100LFM	150LFM	250LFM	System Dependent

Table 36 Thermal Boundary Conditions Assuming Cold Aisle Containment

9. FRU Requirements

The RunBMC module will make use of multiple FRUs. A system that uses the RunBMC module shall provide a FRU on the system board for access from the module. The module shall provide a FRU that contains identification of the module on the I2C9 bus, and the SoC on the module should be addressable as a bus slave on the I2C9 bus in normal operation. Factory programming of the I2C Identification EEPROM may be done from the SoC (as bus master) prior to use in the system.

FRU	Description	Location	I2C BUS	I2C address
I2C Identification EEPROM. Identification field can be programmed in “M/B Custom Field 1”	EEPROM used for FRU data, system purposes, identification. Motherboard designers should allow access for the HOST SMBus to access identification FRU on I2C BUS 9.	RunBMC module	9	0xA2, 8bit
I2C Personality EEPROM	EEPROM used by SOC to define personality of system	System Board	4	0xA0, 8bit

Table 37 RunBMC FRU Requirements

It is recommended to use a minimum size of 2 Kilobytes for Serial Accessed EEPROM on the SMBus. Two of the fields in the Identification EEPROM define the MAC Addresses of the BMC SoC, the addresses of these fields can be found in the Table 38. For further reference and information of the Identification EEPROM should be programmed, see the IPMI V2.0 Spec, Table 11-1 Board Info Area, for EEPROM identification field.

Data	Offset
FRU & Board Info Area	0x0000
BMC MAC1 Address	0x0400
BMC MAC2 Address	0x0406

Table 38 Identification EEPROM fields

10. Platform Guidelines

These guidelines are recommendations that should be heeded in general for any engineer intending to use the RunBMC module.

- BMC programmers should be advised to create a software abstraction layer. This layer will help map the RunBMC connector pinout to SOC pins specific to the vendor module.
- VDD_RGMII_REF is intended to be used as a reference voltage, which is provided by the RunBMC module.
    - As an example, RGMII bus from vendor A module uses 1.8V while vendor B module expects 3.3V. The module designer can use this reference voltage to set the IO voltage level on the PHY, if it supports this functionality.
- VDD_LPC3V3_ESPI1V8 is an input to the LPC or ESPI function. LPC expects 3.3V on this signal and ESPI expects 1.8V.

11. References

- Registration - 260 Pin DDR4 SODIMM, 0.50 mm Pitch. DIMM; M0-310C, Item No. 11-14-164
- Registration - DDR4 Small Outline Dual Inline Memory Module (SODIMM), 260 pin, 0.50 mm pitch Socket Outline; SO-018D, Item No. 14-180
- NXP Semiconductors. *I^2C-bus specification and user manual.* NXP Semiconductors, Rev 6, April 4th, 2014.
- EEPROM identification field, IPMI V2.0 SPEC, Table 11-1 Board Info Area