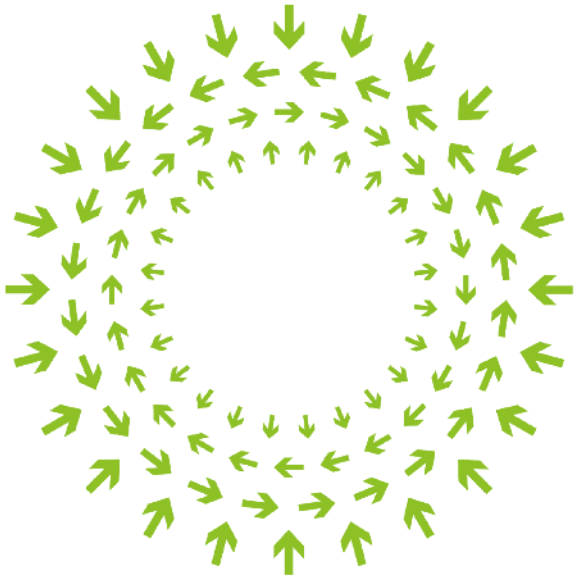

OPEN Compute Project

Open Rack V3 48V BBU

Rev: 1.4

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The Contributors of this Specification would like to acknowledge the following companies for their feedback:

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Revision History

Revision	Date	Description	Author
0.1	2020/03/25	First draft	David Sun
0.2	2020/04/10	Updated thermal, mechanical, compliance and reliability/quality sections	Cheng Chen, Chenyu Xu, Ben Kim, Rommel Mercado
0.3	2020/04/30	1. Section 4.4 Charger minimum input voltage changed from 47.5V to 48.5V 2. Section 8.4 Latch position is on the top side of BBU 3. Section 8.5 Corrected input/output connector PN.	David Sun Chenyu Xu
0.4	9/29/20	1. 4.3 Change discharger output voltage setting and droop to 48V@0% and 47V@100% load to keep >2V voltage gap with PSU. 2. 4.3 BBU minimum life 4 years->8 years 3. 4.3 Add surge load requirement same as PSU. 4. 4.5 Change BBU output activation and exit thresholds. 5. 4.5 Add BBU/PSU output voltage gap tolerance analysis as attachment. 6. 4.16 Add connector pinout table	David Sun
0.5	10/07	1. 4.16 Updated connector pinout table 2. 8.1 Mechanical dimensions 3. 8.2 Updated table of LED indicators 4. Added V3 PMC/PSU/Power Shelf specs in Appendix.	David Sun Chenyu Xu
0.6	11/19/20	1. 4.16 Add SOH pin to avoid more than one BBU SOH test. 2. 4.16 Reverse the logic of BBU BKP_RED. 3. 8.5 removed “R/A plug” to avoid confusion 4. 4.16 Updated I2C_SDA and I2C_CLK connection per PMI/PMC spec Rev 0.67	David Sun

0.8	5/26/21	**FOR EVT build** **4.3** Discharge time changed from 300s to 240s. Battery pack changed from 12s6p to 11s6p and discharger input voltage range changed accordingly. Discharger output voltage setting changed to 47.5V@100%, 47.75V@50%, 48V@0% load. Droop changed to 0.5V from 0% to 100% load. Discharger maximum output current 62A->63.2A (i.e. 3KW@47.5V) Added 240s requirement at PCM threshold as worst case (e.g. 3.9V/cell). Maximum output capacitance 20mF per shelf. 4.3.1 Updated peak load requirements. 4.3.2 Added overload behavior 4.3.3 Added forced discharge mode for peak power shaving 4.3.4 Added forced BBU detached mode **4.4** Charge current ripple +/-1% ->+/-100mA 4.4.1 added variable charge current control 4.4.2 added charge current override 4.4.3 added charge current at various work modes **4.5** Modified PSU/BBU power transition thresholds and added diagram. **4.6** Added more details for SOH test: 1500W(>500W) constant power discharge, >90s remaining capacity, SOH_L signal, SOH proceeding/not proceeding conditions and detections (CANBUS, SOH_L, Modbus), SOH accuracy, etc. **4.7** Removed programmable droop (1%-5%) requirement. Droop is 0.5V. Added share bus voltage requirement: 7V@100% load, 10.5V@150% load. **4.10** Added description of permanent failure and request of fault detect/clear/action details for all faults. **4.12** Constant current operation deleted. Updated Table6 signals pull up/down connections. Updated I2C/Modbus pins assignment and connection per PMI spec Rev0.52.	David Sun Ben Kim Dmitriy Shapiro Jayati Athavale

		Added CANBUS pins CAN+/-. Added SYNC_STOP_L pin. **4.13** Added signal description section Vout_SEL 50V->51V **4.14** Added health check button **4.15** Added BBU shelves parallel operation **5.1-5.4** Updated Section5 Communication and firmware requirements. Added sensors accuracy. **6.5** Updated shock & vibe requirements **6.6** Added packaging requirements. **7.10** Maximum exhaust air temperature 70C->55C **8.1-8.11** Updated entire mechanical section. **8.2** Separated LOV and EOL LEDs **8.4** Added LOV LED threshold SOC<30% **10.1** Added UL9540/9540A and IEC62619 requirements **10.1.1** BBU module shall not explode or spread fire when battery cells undergo thermal runaway condition. BBU shelf shall not explode or spread fire when battery module undergoes thermal runaway condition. **10.2** Deleted VCCI, KN 32 and KN35; changed ESD spec to 5.6kV contact and 11.2kV air.	
0.9	7/28/21	**4.1** BBU sleep mode exiting threshold adjusted to ≥46V 100ms. **4.3** Maximum output capacitance 20mF -> 60mF per shelf to match with PSU spec. Step load requirements updated. **4.4** Adjusted charger CV mode output voltage to 44.1V+/-0.1V. **4.13.1** RS485+/- 120Ω terminating resistor. **4.13.8** BBU 48Vsense+/- connection to shelf output connector. **5.1** SOH accuracy +/-3% TBD based on the BBU 3.45KW (+115%) 90s peak load evaluation. **6.4** Acoustic 55dBA ->85dBA **8.1:** Updated view to include new front features, new connector bracket/dimensions **8.4**: New section regarding health check button	David Sun Dmitriy Shapiro Jayati Athavale Ben Kim

		8.5 Added LOV LED threshold SOC<30% **8.6**: Updated handle drawing and details on handle attachment **8.7**: New section **8.9**: Updated drawing **8.10**: New section **8.11:** Updated drawings	
0.91	9/10/21	**4.1** Set Sleep Mode wake up time upper limit 200ms. **4.3** Discharger output total regulation upper limit 49V->49.5V **4.3.4** Modified description of Detached Mode. **4.4.1** Variable charge current minimum 1A and modified I-E chart. **4.6** Added description for SOH minimum 500W discharge power. **5.2** Default Modbus baud rate from 115K to 19200.	David Sun Dmitriy Shapiro Jayati Athavale Ben Kim
0.92	9/13/21	**4.4** Charger minimum input from 48.5V to 49V, maximum input current 5.5A->5A; maximum input power 275W->250W. **4.5** Updated Figure2 Transition between Power Shelf and BBU Shelf **5.1-5.2** Moved register maps to a separate document (V3 BBU Modbus Register Map Rev 0.4). **8.1, 8.4, 8.11** Changed wording under health check button from HEALTH to CHK	David Sun Dmitriy Shapiro
0.93	1/14/22	**4.1** Storage time >1 year at 30% shipping SOC **4.3** Discharger max current 100A->110A **4.4** Added Max charge power 130W@2A; 265W@5A; Maximum recharge time 6 hours from 0% to 100% SOC at 2A per battery pack. 4.4.1 Variable charge current formula change to 1A/2A two steps. 4.4.3 BBU default maximum charge current changed from 5A to 2A. 4.4.4 Added charge delay time 1minute. **4.8** Added requirement for inrush current and single fault **6.1** Added clarification of operation temperature and long-term operation temperature. **6.9** Added Gaseous Contamination spec **7.5** Added Fan Lifetime spec **8.3** Updated material clarification **8.11** Updated drawings with PN	David Sun Jayati Athavale Dmitriy Shapiro Rommel Mercado

		9.2 Updated MTBF requirements **9.4** Updated Burn-in and ORT requirements **9.6** Added E-cap life requirement **11.8** Added "ORV3 BBU CANBUS Specification" and "ORV3 BBU Modbus Writable Registers" in Reference Documents section.	
0.94	3/17/22	4.3.1 Updated pulse power and pulse power width charts per PSU spec Rev0.95. 4.3.2 OCP 160% OCP delay time 10ms to 20ms 4.4 table3 Charger input transient voltage 48.5V to 46.5V for <2ms. 4.7 Added droop sharing accuracy requirement (4X active sharing tolerance). 4.12 Table 4 Added 48V and 48V RTN connection to PMI/PMC edge connector Removed 10K resistor pull up for PLS_L Added BKP_RED_L pull-up and shelf connection Changed RS485_Addr2/1/0 pull-up resistor from 10k to 100k. 4/12/22: 4.6 Updated the table of detection of SOH conditions. added SOH precheck conditions statement for multi-shelves daisy chain configurations. 4/21/22: 4.4.1 Added note2 for setting charge current at 2A when RSOC falls below 50%. 5/3/22: 4.14 table 4 and 4.13.4 change name of PSKILL_L signal to PSKILL 7/6/22: 4.1 Table1 added standby mode total power consumption requirement. 7/7/22: 4.3.2 Updated over current protection 4.3.3 updated forced discharge section 4.3 Table2 maximum capacitance 60mF/shelf. 7/8/22: 4.3.3 added 3 seconds delay time before existing discharge mode. 4.6 Added requirement to cover AC loss during SOH test. 7/22/22: 4.13.14 added SYNC_START_L reset to high after 100ms in discharging. 7/29/22: 4.6 SOH_L signal and the bit of CANBUS release to high at the end of SOH discharge. 8/2/22: 4.10 Stop fan for permanent failures.	David Sun
1.0	8/15/22	Updated with OCP 2022 spec template	David Sun
1.1	9/1/22	4.4 Charger output CV mode ripple noise +/-1%->+/-0.2%	David Sun
1.2	9/19/2022	4.3, 4.6 SOH boost mode maximum output 51.5V	David Sun

		4.6 SOH precheck condition “No neighboring BBUs” changed to “No BBUs” 4.13.11 BKP_RED_L signal logic reversed. 8.5 EOL threshold default setting for 90s backup time and adjustable by user. Charging mode LED blinking frequency change from 0.5s on/0.5s off to 1s on/1s off.	
1.3	10/26/2022	Added FSC in Acronyms 4.7 Specified SOH discharge delay time within 90s after fully charged. 4.12 Table4 Corrected typo of BKP_RED signal logic. Filled in Appendix A and deleted appendix B	David Sun
1.4	09/12/2023	8.1 Redid views to reflect removal of EMI gasket 8.7 Removed section for EMI gaskets as these are no longer required 8.11 Updated drawings to reflect removal of EMI gasket	Dmitriy Shapiro

1. Scope

This document defines the technical specifications for the Open Rack V3 BBU (Battery Backup Unit) used in the Open Compute Project.

2. Overview

This specification defines the BBU (battery backup unit) that fits into the BBU shelf. The BBU is intended for use in a BBU shelf that is part of the rack for supplying DC power to system loads during AC power outages. 6 BBUs with 5+1 redundancy are included in the BBU shelf.

The BBU operates based on “narrow-range 48V Architecture,” with the output voltage at 47.5V-48V.
The BBU module consists of a battery pack and BMS, charger/discharger and other function blocks as shown in Figure 1.

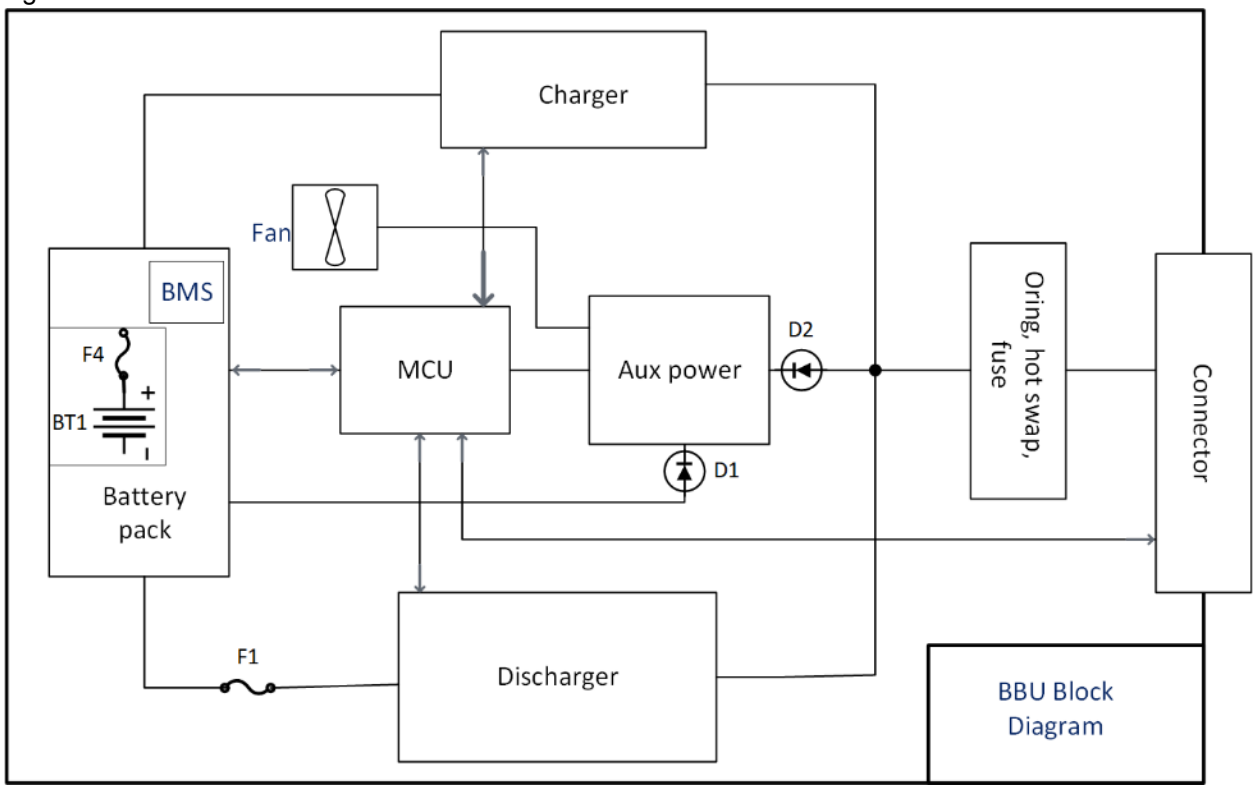


Figure 1

3. Acronyms

BBU: Battery Back Unit
PMI: Power Monitoring Interface
PSU: Power Supply Unit
BMS: Battery Management System
SOH: State of Health
SOC: State of Charge

FCC: Full Charge Capacity
EOL: End of Life
PCM: Periodical Charging Mode
DOD: Depth of Discharge
PLS: Power Loss Siren
FSC: Fan Speed Control

4. Electrical Requirements

4.1. BBU Operation Modes

Table 1

BBU operation mode	**Description**
Sleep mode	When BBU is in transportation or stock or is not attached to an active busbar, the cell discharge current is minimized for longer storage time (>1 year@30% shipping SOC). BBU monitoring/reporting is not available in Sleep mode. The BBU will wake up and exit Sleep mode when the busbar voltage is detected to be above 46V for >100ms and <200ms and PSKILL signal is low.
Standby mode	The BBU is fully charged and healthy, constantly monitoring busbar voltage to be prepared for a discharge event. The BBU operates in this mode for most of its lifespan. The BBU's status and parameters are visible on the upstream rack monitor through the communication bus. The BBU in standby mode total power consumption shall be kept lower than 15W, including fan power.
Discharge mode	When the busbar voltage drops below 48.5V for 2ms (+/-0.1ms), BBU discharge mode is activated. The BBU is expected to take over the busbar voltage within 2ms (TBD).
Charge mode	The BBU enables its internal charger to charge up its battery pack when all conditions are met. The charger current can be anywhere from 0A - 5.5A based on the previous depth of discharge of the battery capacity. It also allows the upstream system to override the charge current through the communication bus. There should be a charger timeout control scheme based on the calculated charge current.
Status of health check mode (SOH)	The BBU routinely tests battery pack capacity through forced discharge of the battery pack. The BBU shall perform the SOH test every 90 days to determine the battery's EOL status. See 4.6.
Periodical charge mode (PCM)	Because the BBU battery pack leaks current in standby mode, it needs to be periodically recharged. See4.4.4.
Fault mode	In fault mode, the BBU is not allowed to charge/discharge and should be replaced as soon as possible.

System control mode (e.g. forced discharge mode, forced detached mode, etc.)	The BBU shall allow upstream system to control charger/discharger operation through communication bus.
Health Check mode	While the BBU is in sleep mode, after pressing “CHK” button, BBU will report its status through LEDs for 10s then goes back to sleep mode. See 4.14.

4.2. Battery Pack

There is a battery pack installed inside the BBU with a mechanical assembly.

4.2.1. Battery Pack Capacity

The battery pack shall enable BBU to provide 3KW discharge power for ≥4 minutes with battery voltage at PCM threshold (e.g.3.9V/cell) over a period of ≥4 years at 35degC (the maximum BBU ambient temperature for long term operation).

4.2.2. Battery Cell Type

A Li-ion battery is considered suitable for this high discharge rate and high energy density application. The reference battery cell in this spec is 18650 type with the min 1.5Ah, 3.5V-3.7V nominal, 4.2V max, 30A max continuous discharge current.

4.2.3. Battery Pack Configuration

Based on the reference battery cell type in 4.2.2, the recommended configuration of the battery pack is 11S6P (6 parallel strings of 11 cells in series each string).

4.2.4. BMS

The BMS shall include a protection mechanism and logic circuitry to generate and control algorithms and signals used in the BBU.

The BMS shall also include a cell balancing circuit where the cell voltage on all battery cells in a pack are kept within +/-1%. The BMS shall provide system monitoring and control functions through the communication bus.

The BMS shall support other functions such as SOH, SOC, PCM, failure events log, remote FW upgrade, etc.

4.3. Discharger

There is a 3KW Discharger in each BBU module. The Discharger characteristics are defined in Table2 below.

Table 2

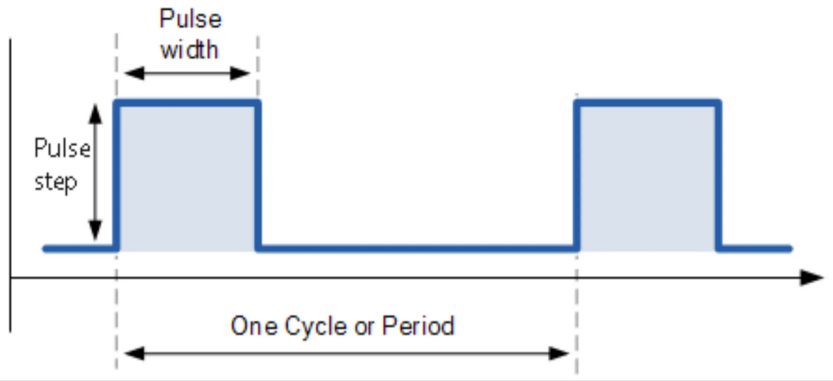
	Min	Typ.	Max	Peak	Unit	Note*
Input voltage	28.6* (2.6V/cell)	-	44.0* (4.0V/cell)	-	V	Assuming 11S6P 18650 Li-ion
Input current	-	-	110	TBD	A	
Output voltage setpoint	47.70	47.75	47.80	-	V	@50% load
Output voltage	47.9	48.0	48.1			@0% load
Output voltage	47.4	47.5	47.6			@100% load
Output voltage total regulation	46.0*	47.5	49.5*	-	V	Including load transient

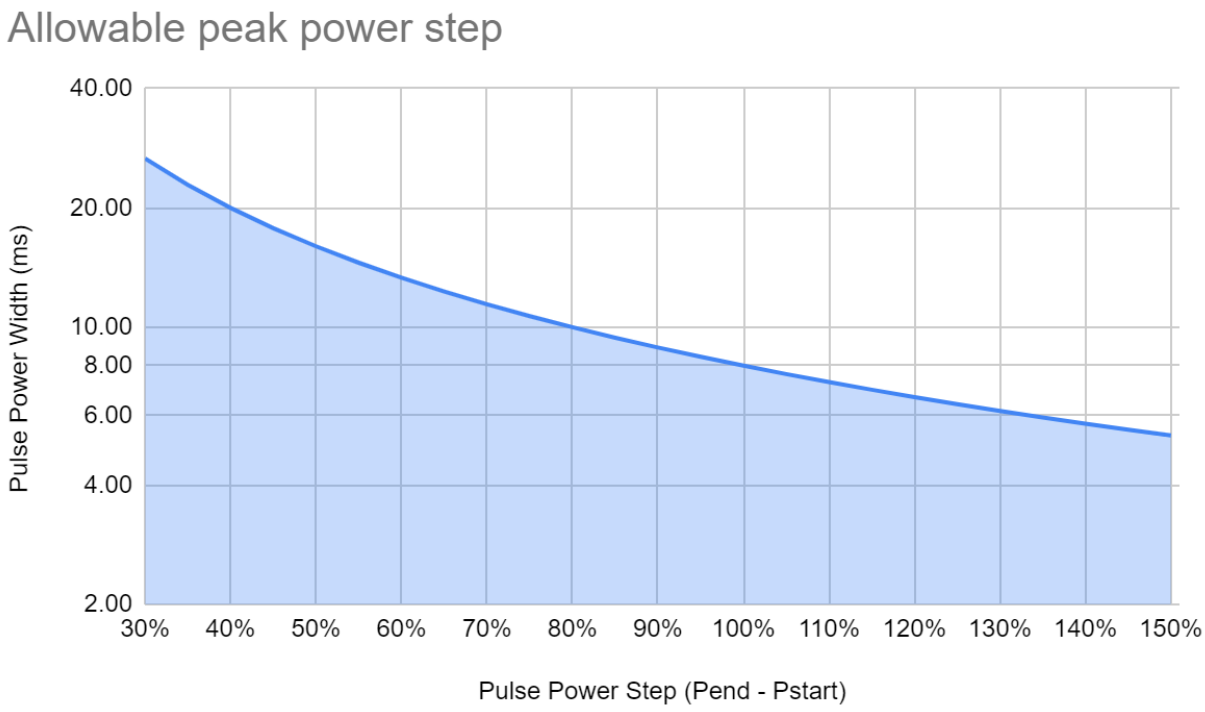
Output voltage droop	0.45	0.5*	0.55	-	V	Output voltage droop 0.5V(1%) from 0% load to 100% load
Output voltage boost limit for SOH	-	-	51.5*	-	V	BBU boost voltage up to discharge energy at CP mode (e.g.1.5KW)
Output current	0	-	63.2	*	A	See 4.3.1 peak load
Output power	0	-	3,000	*	W	See 4.3.1 peak load
Output capacitance	0	-	60*	-	mF	Maximum capacitance per shelf
Battery backup time	240*	-	-	-	seconds	Full power discharge time @≥3.9V/cell.
BBU life	8*	-	-	-	years	Full power discharge time >240s at PCM threshold (e.g.3.9V/cell) ≥4 years @35degC
Output ripple voltage	-	-	300*	-	mVpp	Peak to peak
Transient load response	-3%*	-	+3%*	-	-	1. Step load 0%-80% with 0.1A/µS slew rate, 2. Step load 80% with 1A/µS slew rate @≥10% load, 3. Minimum voltage shall be >46V at any dynamic load conditions including peak power step (4.3.1, 20%-150%, 1A/us).
Startup time	-	-	2*		ms	From discharger activation to BBU output voltage and current fully ramp up including peak load condition (150%).
Efficiency	97%*	-	-	-	-	1. Minimum efficiency shall cover max load within full input voltage range. 2. Fuse/Hot swap/Oring shall be included if used.

4.3.1 Output Peak Power

The BBU shall meet the following surge power requirements.

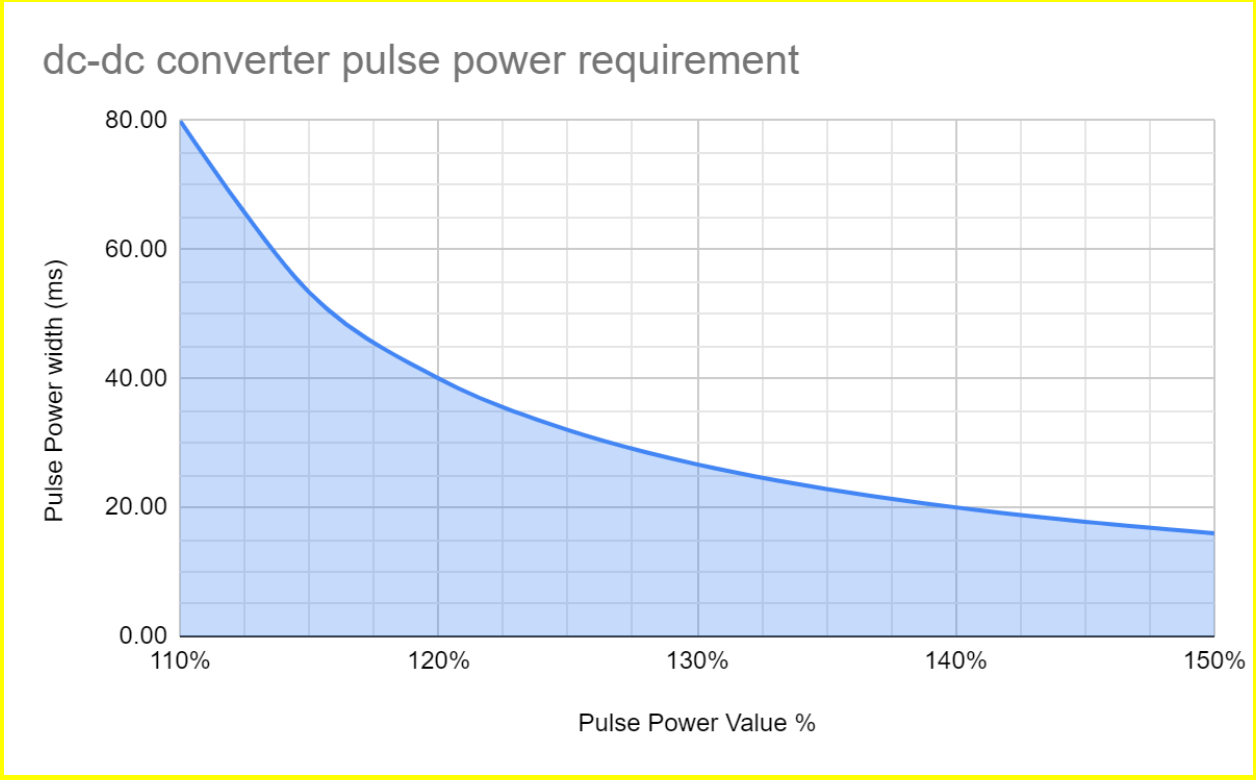
4.3.1.1 Repetitive Peak Load





Note:
1. Absolute maximum magnitude is 150% of BBU maximum output power.
2. Average output power of BBU including peak load shall not exceed 100%.
3. Peak load frequency is TBD.
4. Minimum load before peak load step is 20%(TBD). Slew rate 1A/us.

In order to meet the Pulse power requirements as the graph above, the dc-dc converter should meet the following absolute pulse power requirement as shown below. This graph comes from the worst case of Pstart as 100%.



4.3.1.2 Single Non-repetitive Peak Load
Single pulse power shall be more than ORv3 PSU holdup time at the overload condition (up to 150% load).
Refer to pulse power width versus pulse power chart above.

4.3.2 Overload Behavior
The output voltage droop shall linearly extend to the peak load, e.g. Vout=47.25V@150% load.
BBU over current protection shall allow the shelf to power up and deliver full power at worst case non-redundant configuration (e.g. 5+0 or 11+0 for two shelves), including peak power and transition from PSU to BBU.
BBU shall be self-protected for any overcurrent and/or short circuit conditions.
BBU shall set multiple protection levels and delay time for over current and short circuit protection properly. If latch mode over current protection is used, then BBU should retry 5 times before latch off.
The OCP settings should be reviewed by Meta.
100% load =63.2A

4.3.3 Forced Discharge Mode/Peak Power Shaving Mode
This feature can be used for datacenter peak power shaving.
Starting procedures:
Rack Monitor sends Modbus forced discharge commands to PSUs and BBUs including forced discharge time duration.
BBUs start and increase output voltage by 3V to 51V-50.5V (0.5V droop from 0% to 100% load).
PSUs reduce output voltage by 3V to 48V.

Exiting procedures:
The forced discharge will end in the following scenarios: 1) Forced discharge time register is expired; 2) Rack Monitor disabled forced discharge; 3) BBU remaining capacity falls below 120s (TBD).
For scenarios 1&2,
PSUs raise voltage back to the normal range 51V-50.5V
BBUs exit forced discharge mode and reduce voltage by 3V to 48V for around 3s. After 3s, if BBU detects bus voltage >48.5V for >200ms, then BBUs exit discharge mode and enter standby mode.
For scenario 3,
BBUs exit discharge mode when remaining capacity is below 120s (TBD).
If PSUs detect bus voltage <50V for >10s, then the PSUs will raise voltage back to normal.
Sync_Start_L/Sync_Stop_L shall be used for BBUs simultaneously entering and exiting from forced discharge mode in order to avoid BBU over current protection due to start/stop time difference.

4.3.4 Forced Detached Mode

Rack Monitor can use Modbus command to temporarily disable BBU discharge function to allow remote rack power cycling to reboot all servers.
The command shall be used with a programmable timeout(0x134) with a default value of 30 minutes.

4.4. Charger

There is a Charger in each BBU to charge up the battery pack. The Charger characteristics are defined in Table3.
Table 3

	Min	Typ.	Max	Unit	Note (*)
Input voltage	49*	50.5V-51V	53	V	Charger shall accept busbar transient voltage below 49V and above 46.5V for <2ms.
Input current	0	-	5	A	CC/CV mode charge and adjustable CC charge current
Input current overshoot			10%		
Input power	0	-	250	W	
CC mode output current	0	*	5	A	The charging current is a variable based on previous discharge level.
CC mode output current tolerance			+/-0.1A		
CC mode output ripple current	-100	-	+100	mA	Peak-peak
CV mode output voltage	44.0*	44.1*	44.2*	V	Voltage at no load to 0.5A load
CV mode output ripple voltage	-0.2%	-	+0.2%	-	Peak-peak at no load to 0.5A load
Efficiency	95%*	-	-	-	Fuse/Hot_swap/Oring shall be included.

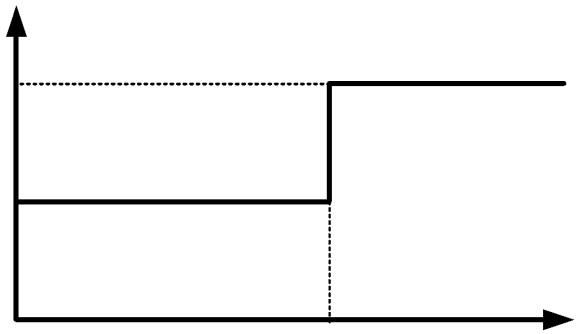
Charge Power			130W@2A * 265W@5A *	W	Total BBU input power drawn from busbar including fan and control circuit. 2A/5A is battery pack input current.
Charge time	-	3*	6	hours	Maximum recharge time from 0% to 100% SOC) at 2A per battery pack

4.4.1 CC Mode Variable Charge Current

The BBU battery pack CC mode charge current is set based on the following formula and chart:

Battery Pack Charge current(A) $= \{1,\ EOD < 200kJ\ 2,\ EOD \geq 200kJ$

EOD is BBU discharged energy in kJ.



Note:

1. The Variable Charger approach is intended to decrease the charge current and therefore power in a data center application where there may be thousands of BBUs requesting charge at the same time. Once calculated, $I_{Charge\ Target}$ value is to be written to register 0xA0 so that it can be read through Modbus.
2. Battery pack charge current should be set at 2A when RSOC falls below 50% in order to keep maximum charge time within 6 hours.

4.4.2 CC mode Charge Current Override

Rack monitor can override BBU CC mode charge current from 0 to 5A through Modbus commands. The BBU should not assert any failures as a result.

The BBU is to allow charge sequence to be skipped or delayed. 0A signifies a charge delay.

4.4.3 BBU Charge Current at Each Different Charge Mode

BBU Charge Mode	Charge Current	Charge enable (PCM) Threshold

Initial shelf power up	2A	3.9V/cell
BBU installation	2A	3.9V/cell
Recharge after SOH	2A	3.9V/cell
AC loss/ Busbar voltage <48.5V@>2ms	0xA0(calculated variable charge current) or 0X123(Override current)	3.9V/cell
PCM	2A	3.9V/cell

4.4.4 Periodical Charging Mode

Because the BBU battery pack leaks current in standby mode, the battery pack needs to be periodically recharged. It is called the 'Periodical Charging Mode'. The PCM is set between 3.9V and 4.0V per cell (42.9V to 44V of battery pack output voltage). The amount of current leaking from the standby mode battery pack to the BMS, discharger, etc. shall be minimized. If there are no discharge sequences, the BBU should recharge the battery pack no more than once every 10 days.

4.4.4 Charge Delay Time

After a BBU discharge event, the BBU shall delay charge sequence by 1 minute for system to set the overriding charge current when needed.

The BBU may need longer time for cell to cool down before charge starts.

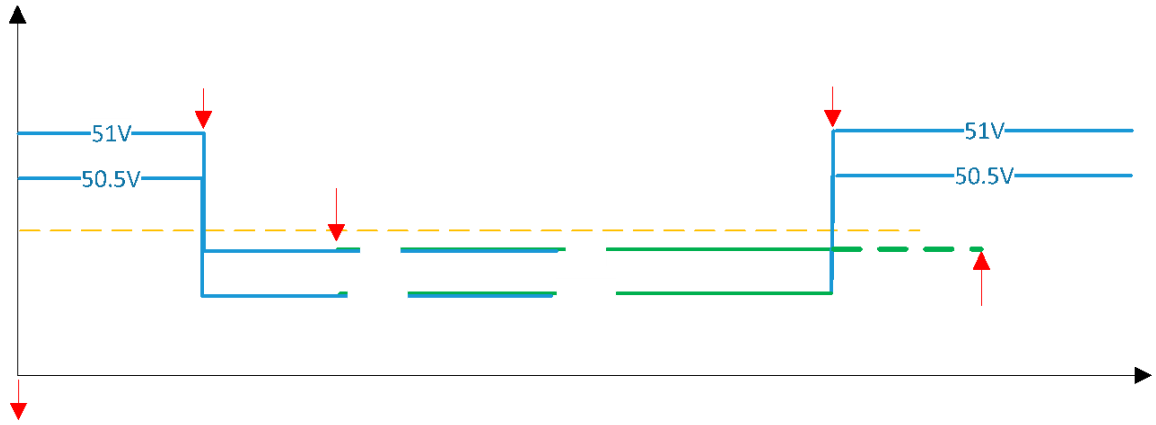
4.5. Transition between Power Shelf and BBU Shelf

BBU shall constantly monitor busbar voltage. When the busbar voltage declines to the BBU activation level 48.5V for 2ms+/-0.1ms (TBD), the BBU shelf output voltage shall ramp up to provide full power to the busbar within <2ms. During the transition, the busbar voltage shall never drop below 46V.

When the BBU shelf detects that the busbar voltage is above 48.5V for >200ms (TBD), the BBU shelf exits discharge mode.

PSU/BBU Power Transition Diagram

Figure 2



4.6. SOH test

The BBUs inside a BBU Shelf shall perform a SOH test every 90 days to determine the battery's EOL status.
A random number is generated in the BBU production line and stored in the EEPROM (0x127, range: 0-2159; unit: hour). This is to be associated permanently within each BBU shipped. After the BBU exits the 'Sleep Mode', a clock timer included in the BBU logic starts to count down the hours in the 'First SOH Timer'. Once the countdown has reached its end, the BBU logic will conduct the first battery test (SOH Check) when a set of conditions are met.
Only one BBU inside a BBU Shelf should perform the SOH test at a time. SOH_L signal is used to avoid multiple BBUs in a shelf conducting SOH tests simultaneously. BBU should only proceed with SOH test when SOH_L signal is high. SOH_L signal should be held low during the SOH discharge. At the end of SOH discharge, The BBU releases SOH_L signal to high and de-asserts SOH_L bit of CANBUS.
The BBU SOH discharge shall start within 90 seconds after being fully charged (4.0V /cell). During discharge, the BBU shall increase its discharger output voltage up to 51.5V in order to share a constant power load (e.g. 1.5KW) from the power shelf.
The SOH discharge power shall be kept ≥500W for better SOH result accuracy. During SOH discharge, if rack power falls below 500W then BBU should abort the SOH result and retry one month later. After successful SOH, the subsequent SOH test interval shall return to the standard SOH interval of 90 days. The chance of rack power <500W is extremely low.
The SOH DOD (depth of discharge) shall be defined to allow BBU to back up a minimum of 90s 3KW discharge during and/or right after SOH discharge in terms of remaining capacity and cell temperature. The purpose is to keep 5+1 BBU redundancy for ≥90s backup time in case an AC power outage occurs during or right after SOH.
If AC power outage happens during SOH, due to constant power control, the SOH BBU shall drop its output voltage to <48.5V along with PSU and the rest of the BBUs are activated to deliver power to busbar. The SOH BBU shall stop SOH test immediately and resume normal discharge.
SOH shall only proceed if all the following conditions are met, otherwise, the BBU shall queue the SOH test.

a) No another BBU in SOH test
b) Full configuration of BBUs in the shelf
c) No failed BBU in the shelf
d) No BBU(s) EOL
e) No BBU in firmware update mode
f) All BBUs are in standby mode
g) All BBUs are fully charged or above the PCM threshold (3.9V/cell).

Detection of the above conditions:

Conditions	**Detection**
No failed BBU in the shelf	CANBUS
No BBU(s) should be reporting EOL in the shelf	CANBUS
All BBUs should be fully charged or the BBU cell batteries meet the required voltage limit	CANBUS.
Full configuration of BBUs in the shelf	CANBUS and Modbus 0x133(BBU shelf configuration)
No another BBU in SOH test	SOH_L signal and/or CANBUS

The above SOH precheck conditions apply also to muti-shelves configurations, provided that CANBUS communication between shelves works normally.
SOH queue:

- If a BBU is in queue for SOH test, the blocking conditions can be checked every x minutes (suggested to use 10 minutes) to see if all the conditions are valid now to start the SOH.
- During startup of the BBU shelf a 1-minute delay should be added to avoid a SOH at first turn on.

- If multiple BBUs are in queue at the same time, the priority of the battery tests should be first in first out (FIFO).

The result of SOH and associated timestamp shall be saved in non-volatile memory, refer to register map.
The target SOH accuracy is +/-3% of designed FCC (full charge capacity).
The BBUs shall be able to back up the rack power in case of AC loss when a BBU is in SOH mode.

- When a BBU enters SOH mode, all the rest of BBUs shall also enter discharge mode.
- Byte 0 Bit 4 SOH_L CAN information can be used by the other BBUs to determine that a BBU is in SOH discharge mode.
- The BBUs' maximum discharge time should be disabled when the BBUs are discharging due to a BBU SOH test in the shelf
- The other BBUs will exit the discharging mode when there's no more BBU in SOH mode and verifies that the BUS voltage is good
- At the end of SOH discharge mode, the BBU de-asserts SOH_L bit of CANBUS then all BBUs follow the normal discharge exit criteria.
- In SOH mode without AC loss, PLS_L shall not be asserted. If AC is lost during SOH test, PLS_L should be asserted after BBUs discharge more than 45s (programmable by Modbus register 0x122). The AC loss during discharge mode can be detected by bus voltage and/or BBUs' discharge current.

4.7. Current Sharing and Redundancy

The BBU shall have a dedicated analog bus for active current sharing. With up to 6 BBUs in a shelf, the current sharing accuracy shall be +/- 3% or better under load > 90% and +/- 5% or better under load > 25%. For loads less than 25% of rated output the share shall be 5% of the full rated output power.
The current share bus voltage is 7V at 100% load,10.5V at 150% load, and the current share bus voltage is linear from 0% to OCP threshold.
There is a 0.5V output voltage droop from 0% load to 100% load. The same slope of output voltage droop extends to the OCP threshold.
In the event of Active current sharing getting broken, the BBU shall share the load through voltage drooping with accuracy up to 4 times the values above. The failure of a module inside the BBU should not affect the load sharing or output voltages of the other supplies still operating. The supplies must be able to load share in parallel and be able to hot-swap.

BBU shelves current sharing requirements are defined in 4.15.

4.8. Redundancy and Hot Swap

The BBU is hot-pluggable to a live BBU shelf.
The BBU shall have an Oring device on each output for N+1 redundancy for parallel operation and redundancy.
To avoid bus voltage glitch at BBU/Shelf hot plug, there should be no capacitors placed on the shared voltage bus after Oring devices either in the BBU or shelf.
Hot-swap or similar circuits are needed on any circuits connecting to busbar voltage to avoid busbar voltage disturbance at hot swap and component single fault.
When the BBU shelf is discharging, a newly inserted BBU shall wake up and discharge along with other BBUs.

4.9. Fuse

Fuses are necessary to protect against catastrophic failures and safety hazards. For example, fuses should be placed at the following locations: 1) between battery pack and discharger input, 2) on charger input, 3) on Aux converter input, etc.
There should be a controlled fuse between the charger and battery pack to protect against charger faults such as OVP.
Fuses should be properly rated for maximum operation current and short circuit interrupting current.
The status of main fuses shall be monitored and reflected in BBU status registers.

4.10. Protections

The BBU shall protect battery pack, charger and discharger from damage under the following fault conditions
Battery pack over charge
Battery pack over discharge
Over current
Short circuit
BBU/BBU Shelf output short circuit during discharge and standby mode
Over temperature
Over voltage
Under voltage
Other faults
The following failures are permanent. Once the permanent failure is detected, the failure cannot be cleared by MCU reset and the BBU is permanently in fault mode, no charge/discharge, fault LED on. BBU fan should shut down in case of a permanent failure listed below.
Cell voltage ≥4.23V
Cell voltage ≤2.0V
Cell temperature ≥85C
Battery pack charge FET failure
Battery pack charge/discharge fuse blown
Battery pack charge timeout
Cell balancing failure
Other permanent faults
BBU supplier shall provide all faults/protections detect/clear thresholds and actions for review.

4.11.Interoperability

The BBU modules, PMIs and BBU shelves from different suppliers shall be interoperable and interchangeable in any mixed configuration.

4.12. BBU Connector Pinout

Figure 3

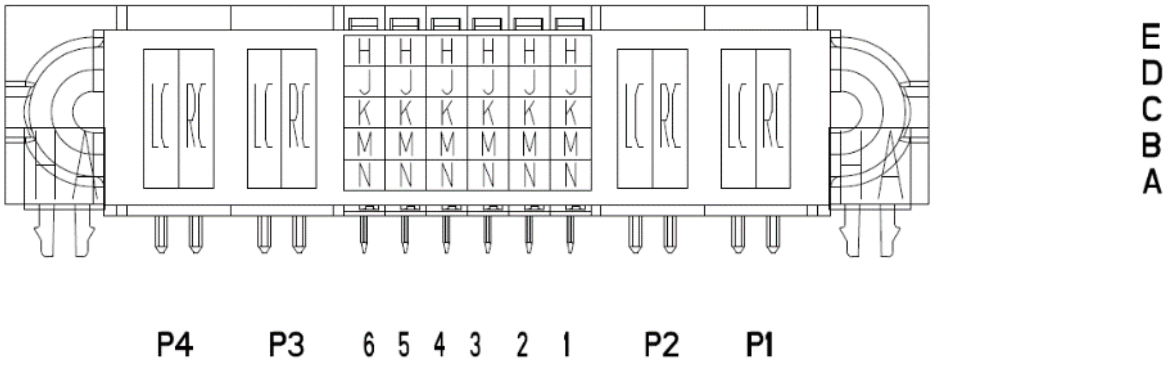


Table 4

Pin Number	Pin Name	PMI/PMC shelf edge connector signal name and pin number
P1 & P2	48V return	P48V_RTN(A40, B40)
P3 & P4	48V positive	48V Power In(A42, B42)
Note: P1, P2 mate first and break last.		

Pin number	Signal Name	Type	Function	Pull up/down @BBU	Pull up/down @shelf	Corresponding PMC to shelf edge connector signal name and pin number
A1	RS485+	I/O	Modbus communication		Connected together at shelf then to PMI	RS485A(B18)
A2	RS485-	I/O	Modbus communication		Connected together at shelf then to PMI	RS485B(A19)
A3	A0	Input	BBU Address 0	10K to 3.3V	Ground/open	N/A
A4	A1	Input	BBU Address 1	10K to 3.3V	Ground/open	N/A
A5	A2	Input	BBU Address 2	10K to 3.3V	Ground/open	N/A
A6	A3	Input	BBU Address 3	10K to 3.3V	Ground/open	N/A
B1	SGND			10 Ohm to 48VRTN		GND (B2/A9/B15/B31/A34)
B2	SYNC_STOP_L	Input /Output	Synchronously turn off the main output. Input/Output=low -> Discharger output turns off immediately;	10KOhm to 3.3V; transistor to ground.	Connected together at shelf then to PMI	A31
B3	PSKILL (short pin length)	Input	Quick shut down output to mitigate hot unplug arcing.	10K to 3.3V	10 Ohm to SGND	N/A
B4	N/A					
B5	BBU_ALERT_L	Output	Logic "Low"= BBU not Ready Logic "High"= BBU Ready Ready indicates that BBU can support discharge.	10K to 3.3V		ALERT_0_N(A3) ALERT_1_N(B3) ALERT_2_N(A4) ALERT_3_N(B4) ALERT_4_N(A5) ALERT_5_N(B5)
B6	SGND			10 Ohm to 48VRTN		Same as BBU “B1”
C1	SDA	I/O	I2C data (reserved)	3.3K to 3.3V		I2C_SDA0/1/2/3/4/5(B19/20/21/22/23/24)
C2	CLK	Input	I2C clock (reserved)	3.3K to 3.3V		I2C_CLK0/1/2/3/4/5(A20/21/22/23/24/25)
C3	SGND			10 Ohm to 48VRTN		Same as BBU “B1”
C4	CAN_H	I/O			Connected together at shelf	A30
C5	CAN_L	I/O			Connected together at shelf	B30

C6	BBU_ISHARE	Analog	Active current sharing bus for BBU and shelf.	Analog	Connected together at shelf then to PMI	ISHARE(A32)
D1	N/A					
D2	48V_Sense+	Analog	Remote sense +	Analog signal	Connected together at shelf then to shelf busbar clip	N/A
D3	48V_Sense-	Analog	Remote sense -	Analog signal	Connected together at shelf then to shelf busbar clip	N/A
D4	BBU_Reset	Input	Logic "Low to High for 1s-2s"= BBU reset. Reset means BBU output turns off and on including MCU reset.	10K to SGND	Connected to PMI	RESET_0/1/2/3/4/5(B9/A10/B10/A11/B11/A12)
D5	SOH_L	I/O	Low: BBU in SOH test. If one BBU is undergoing SOH test, the 2nd BBU shall wait until SOH turns high.	10K to 3.3V	Connected together at shelf	
D6	BKP_RED_L	Output	Logic "low"= BBU shelf redundancy lost (i.e. one or more BBU failed) Logic "high"= BBU shelf redundancy OK (i.e. all 6 BBUs are OK) Not used.	open collector transistor to ground.	Connected together at shelf then to PMI	BKP(B16)
E1	VOUT_SEL	Input	Logic "Low"= Set Output is 48V Logic "High"=Set Output is 51V	10k to SGND, Default Output is 48V	Connected together at shelf then to PMI	VOUT_SEL(A33)
E2	PLS_L	Output	Power Loss Siren. Logic low: BBU has been discharged for ≥ 45 seconds due to PSU AC loss. The PLS threshold is configurable by Modbus command 0x122. Logic high: BBU discharge time is <45s.	open collector transistor to ground.	Connected together at shelf then to PMI	PLS(A16)

E3	SYNC_START_L	Input /Output	Synchronously turn on main output. Input/Output=low -> Discharger output turns on immediately;	10KOhm to 3.3V; transistor to ground.	Connected together at shelf then to PMI	SYNC_START(B32)
E4	RS485_Addr2	Input	4.13.2	100K to 3.3V	Connected together at shelf then to PMI	RS485_Addr2(A18)
E5	RS485_Addr1	Input	4.13.2	100k to 3.3V	Connected together at shelf then to PMI	RS485_Addr1(B17)
E6	RS485_Addr0	Input	4.13.2	100k to 3.3V	Connected together at shelf then to PMI	RS485_Addr0(A17)

4.13 Signal Pin Descriptions

4.13.1 RS485+/-

Differential Modbus communication bus. All 6 BBUs are connected on the shelf board together and then connected to the TOR through PMI.
The 120 Ohm terminating resistor shall be located on the shelf board next to the BBU farthest to PMI.

4.13.2 BBU Modbus Address

There are seven BBU address pins BBU_ADD0/1/2/3(A0/A1/A2/A3) and Rack_ADD0/1/2(RS485_ADD0/1/2). These are digital signals that should have internal pull up resistors inside the BBU. On the BBU shelf/PMI/TOR, these pins can be grounded (0) or left open (1) to determine the BBU location.

Table 5 BBU address format

Fixed	Fixed	Rack_ADD2	Rack_ADD1	Rack_ADD0	BBU_ADD2	BBU_ADD1	BBU_ADD0
b7	b6	b5	b4	b3	b2	b1	b0
0	1	X2	X1	X0	Y2	Y1	Y0

BBU_ADDx: hardwired at the shelf
Rack_ADD1, Rack_ADD0: Hardwired at TOR
Rack_ADD2: Hardwired at PMI (pin 6) for daisy-chain purposes.

4.13.3 SGND

This is communication and control logic ground. SGND shall be isolated with power return through a 10 Ohm resistor to avoid grounding current from TOR to BBU shelf through RJ45 communication cable.

4.13.4 PSKILL

This is LMFB short pin for hot swap arcing mitigation. The PSKILL is grounded on shelf board through 10 Ohm resistor to provide quick turn on/off BBU discharger/charger DCDC.

PSKILL is also used to wake up BBU from Sleep mode.

4.13.5 BBU_ALERT_L

This signal is low when BBU is in fault mode that cannot charge or discharge.

4.13.6 SDA/CLK

Reserved I2C signals for SMBUS communication.

4.13.7 BBU_ISHARE

This is an active current sharing bus signal that connects all BBUs together on the shelf. This signal is also connected to PMI for shelf-to-shelf current sharing.
The bus voltage is a linear function of output current. The bus voltage is 0V @0 load, 7V @100% load, 10.5V@150% load.

4.13.8 48V_Sense+/-

These signals are used for shelf output busbar clip voltage detection for BBU/PSU transition as well as BBU voltage regulation feedback.
The BBU 48V_Sense+/- shall be connected to shelf output busbar clip.

4.13.9 BBU_Reset

This signal can be used to reset BBU.

4.13.10 SOH_L

This signal being low means BBU is in SOH test mode.
If one BBU is undergoing SOH test, the 2nd BBU shall wait until SOH signal turns high.

4.13.11 BKP_RED_L

This is a reserved signal that is not currently used.
Logic "low"= BBU shelf redundancy lost (i.e. one or more BBU failed)
Logic "high"= BBU shelf redundancy OK (i.e. all 6 BBUs are OK)

4.13.12 VOUT_SEL

Logic "Low"= Set Output is 48V-47.5V from 0% to 100% load.
Logic "High"=Set Output is 51V-50.5V from 0% to 100% load.

4.13.13 PLS_L

The purpose of this signal is to indicate to the data center that an imminent BBU shelf output off will occur in 45 seconds (TBD). This signal is sent low to TOR switch out of the shelf via pin 2 on the PMI RJ45.
Logic low: The signal is pulled low by BBU(s) have been discharged for 45 seconds due to PSU AC loss. The PLS threshold is configurable by Modbus command 0x122.
Logic high: BBU discharge time is <45s.
SOH test, forced discharge and single PSU firmware boot loading shall not assert PLS_L.

4.13.14 SYNC_START_L

SYNC_START_L signal can be used in conjunction with CANBUS to synchronously turn on all BBU modules in a shelf. When this signal is pulled low by any single BBU or PMI, all BBUs shall turn on immediately. For example, when BBU1 detects busbar voltage below 48.5V for 2ms+/-0.1ms, it will pull low SYNC_START, and all BBUs will ramp up output voltage and fully take over rack power within 2ms.
To ensure BBUs to enter/exit discharge mode properly without malfunction such as enter/exit chasing or lock up in discharge mode, the SYNC_START_L signal should be released to high after 100ms of discharging. It won't affect BBUs' backup function since BBUs won't exit discharge mode until 200ms after bus voltage recovery to above 48.5V.

4.13.15 CAN_H/CAN_L

The BBUs in a shelf are digitally interconnected with a separate internal CAN bus (it does not go out from the shelf) for data exchange between the units, such as battery test priority (SOH), number of BBUs(SOH), BBU status(SOH) and PLS signal generation. If a BBU's internal CAN bus communication fails and cannot receive messages from any of the other BBUs then its fail LED should turn amber. It still allows discharge and charge.

CANBUS can also be used in conjunction with SYNC_START_L/SYNC_STOP_L to synchronously turn on/off all BBUs in a shelf to avoid individual BBU going over current.

4.13.16 SYNC_STOP_L

SYNC_STOP_L signal can be used in conjunction with CAN bus to synchronously turn off all BBU modules in a shelf. When this signal is pulled low by ≥2 BBUs, all BBUs shall turn off immediately. The signal can be used to synchronously turn off all BBUs in the following scenarios: 1) busbar voltage recovers at AC recovery; 2) BBU backup time expires (system configurable up to 240 seconds); 3) BBU is forced to stop discharge by system Modbus commands; 4) peak load shaving timer expires; 5) other.

4.14 BBU Health Check Button

There shall be a health check button on the BBU front panel. While the BBU is in sleep mode, when the button is pressed, the 4 LEDs (BBU OK, EOL, FAULT, Low V) on the BBU shall light up for 10 seconds to indicate the status of BBU according to the LED identification table in Section 8.5.

Refer to mechanical section/drawing for the mechanical requirements of the button.

4.15 BBU Shelves Parallel Operation

BBU shelves shall support parallel operation when more IT load power and/or backup time are needed. The multiple BBU shelves are daisy chain connected through PMI RJ45 connector #3 and #4. The BBU shelves use BBU_ISHARE, SYNC_START_L, SYNC_STOP_L and CANBUS_H/L for parallel operation mode control.

5. Communication and Firmware

The BBUs shall communicate with the PMC/PMI through single Modbus. Please refer to the latest version of V3 Communication Specification and V3 BBU Modbus Register Map for detailed requirements of BBU monitoring and control.
The software interface shall be operational when the BBU shelf is not in sleep mode. The BBU communication interface shall provide the following features.

5.1. BBU Monitoring Registers

BBU shall provide registers for the system to monitor BBU operation. Here is the BBU monitoring register map.

Table 6
(Refer to V3 BBU Modbus Register Map.)

5.2. BBU Control Registers

The BBU provides a set of writable registers which allows Rack Monitor to control BBU behavior by writing into these registers. Here is the list of writable registers.

Table 7
(Refer to V3 BBU Modbus Register Map.)

5.3. Non-volatile Memory

The BBU shall include a non-volatile memory (EEPROM or Flash) used to store permanent data. The following information is to be added in the said memory in addition to the vendor specific data:

- Manufacturer Name
- Manufacturer Model
- Facebook Part Number
- FW revision
- Build Revision: EVT, DVT, PVT
- Manufacture Date
- End of Life status
- Battery test results (SOH, SOH timestamp)
- Random Number for SOH test
- Permanent failures (OT, OV, UV, cell unbalance, fuse, fan, etc. Refer to 4.12 description of permanent failures.)

The BBU shall also store some programmable registers contents in non-volatile memory so that the programmed features stay effective after MCU reset. Refer to V3 BBU Register Map for details of requirements.

5.4. In-system Firmware Upgrade

The communication interface shall allow the user to re-flash firmware of all digital controllers in the BBU. Firmware upgrades shall result in no power interruption on the shelf level (the unit being upgraded can go offline.) Firmware upgrades should be done one BBU at a time. Firmware upgrade time shall be less than 2 minutes per BBU.
The flash/EEPROM shall always keep a working copy of the firmware on the BMS. In the event of a firmware update failure, the BBU can be recovered with a previously stored version of the firmware.

5.5. Failure Event Log

The BBU shall provide a failure event log triggered by all failure conditions. The failure event log data shall be stored on a flash/EEPROM.

6. Environment

6.1. BBU ambient temperature

- Operational: 0°C to +40°C
  BBU shall support normal operation per spec requirements including 4 minutes discharge at full power 3.9V/cell.
- Long term operational: +15°C to +35°C

This is the data center long term ambient temperature that can be used for battery aging evaluation.

- Non-operational: -20°C to +60°C

6.2. Humidity

- Operational**:** 10-90% RH non-condensing
- Non-operational**:** 5-93% RH non-condensing

6.3. Altitude

- Operational: 0-3000m (can be relaxed to 2000m for FB application)
- Non-operational**:** 0-12000m

6.4. Acoustic Noise

- <= 85 dBA at maximum operation point

6.5. Shock & Vibration

The BBU modules shall meet shock and vibration test per EN 60068-2-6 and 60068-2-27 for both nonoperating and operating condition, with the specifications listed below. During operating vibration and shock tests, the BBU shelf shall exhibit full compliance to the specification without any electrical discontinuities.
During the non-operating tests, no damage of any kind (included physical damages) should occur, and they should not corrupt the functionalities of the BBU per the specifications.

- VIBRATION
  - Operating: 0.5g acceleration, 1.5mm amplitude, 5 to 500 Hz, 10 sweeps at 1 octave/minute per each of the three axes (one sweep is 5 to 500 to 5 Hz)
  - Non-Operating: 1g acceleration, 3mm amplitude, 5 to 500 Hz, 10 sweeps at 1 octave/minute per each of the three axes (one sweep is 5 to 500 to 5 Hz)
- SHOCK
  - Operating: 6g, half-sine 11mS, 5 shocks per each of the three axes
  - Non-Operating: 12g, half-sine 11mS, 10 shocks per each of the three axes

6.6. Packaging

Packaged unit must satisfy test requirements stated below.

Table 8

Package Vibration	1.146 G_{rms}, 2-200-2 Hz, all three axes, Random Vibe	ISTA 3E 06-06
Package Drop	8-inch drop	ISTA 3E 06-06
Package Compression	Maximum compression loading on a bulk pack	ASTM D 642-94

6.7. UN compliance

The BBU shall meet shock, vibration and drop requirements specified in UN38.3, UN3480/81 (transportation safety test requirements) and safety certification requirement.

6.8. Rack level shock and vibration

The BBU and shelf shall be able to meet Facebook rack level shock and vibration requirements.

6.9 Gaseous Contamination

The BBU shall meet Severity Level G1 per ANSI/ISA 71.04-1985.

7. Thermal

7.1. Thermal Design Requirement - Standby Mode

The thermal design of BBU should be able to keep cell temperatures low enough in the long-term standby mode while complying with environment conditions defined above to ensure meeting lifetime and EOL capacity requirements. The design should be optimized so that the airflow and fan power consumption in standby mode is minimized.

7.2. Thermal Design Requirement - Discharge Mode

The thermal design of BBU should be able to support discharge mode operation with the cells at EOL, for at least 4mins, with max output power and worst-case operational environment condition defined above.

7.3. Thermal Design Requirement - Charge Mode

The thermal design of BBU should be able to support charge mode operation at the worst-case operational condition defined above. It should also be able to accelerate the cooldown of cells after discharge and enable recharge within 30mins in the worst-case condition. The FSC (Fan Speed Control) should be designed to control airflow and fan power consumption based on actual cooling needs.

7.4. Airflow Direction

The BBU shall provide an air intake from the front side and exhaust to the rear side to allow front to rear forced convection cooling. The air removal device (fan) should be able to maintain the airflow direction and sufficient airflow rate for cooling with up to 0.05InH2O extra back pressure behind the BBU.

7.5. Fan

Mounting of the fan must meet any vibration and acoustic criteria and will not violate any physical constraints outlined. The fan shall be included within the BBU enclosure. Fan shall not exceed 60x60x38mm. Perforation for the fan shall be made on the front panel. The fan should have L10 spec of 8 years (70,000 hours) at 40C temperature.

7.6. Fan Failure

If a fan fails, the BBU must indicate the failure with a signal that will be reported via SW as well as an LED indicator on the front panel. The BBU shall shut down at fan failure if there is no redundant fan.

7.7. Temperature Sensors

The temperature sensors shall be chosen to meet the monitoring requirements and the accuracy for the sensing is within a +/- 2.0C tolerance. The temperatures of inlet air, exhaust air, hottest cell(s) and other hotspots should be reported.

7.8. Fan Speed Control

The fan speed control should be a combination of multiple control tables (linear or PID) based on inlet temperature, hottest cell temperature, rectifier hotspot temperature(s) and operation mode. It should be tuned properly to support cooling needs of all operation conditions, maintain appropriate thermal margins, reduce unnecessary consumption of airflow rate and fan power, and minimize fan speed oscillation.

7.9. BBU Thermal Monitoring

Each BBU shall provide the following parameters via the defined communication protocol. The following thermal parameters must be available for each rectifier and labeled accordingly:

- Inlet temperature
- Exhaust temperature
- Cell temperature sensors, maybe multiple sensors to capture hottest cells
- Fan speed reading (include all fan/rotor speeds if more than 1 rotor), percent is acceptable as long as full speed rpm is provided at some point.
- Hotspot temperatures on the rectifier
- Fan fail signals
- Component overheat signal

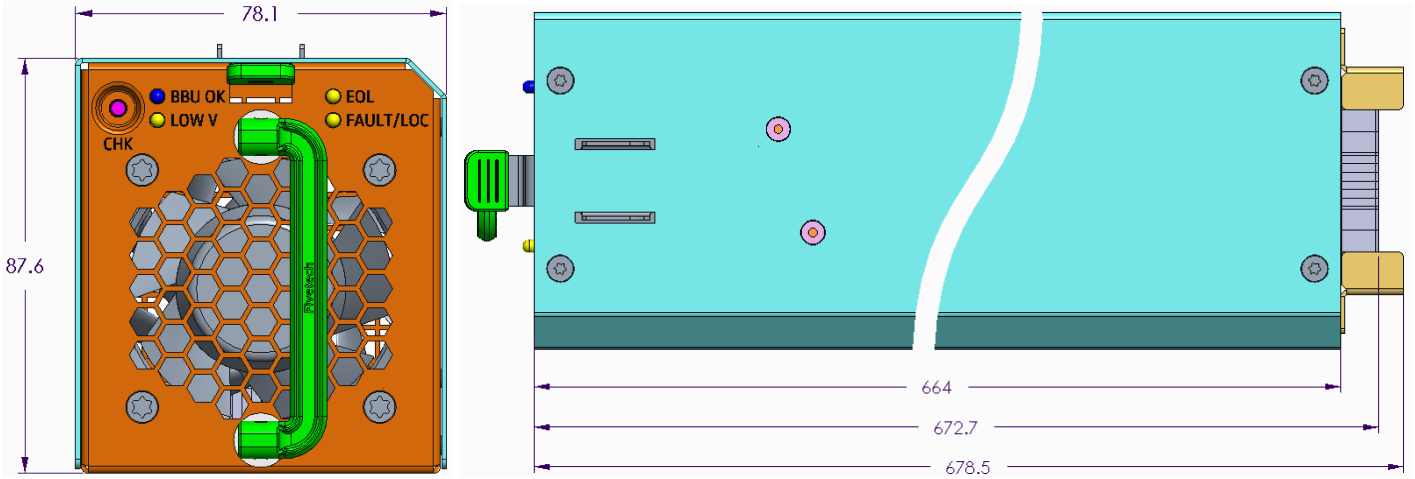
7.10. BBU Exhaust Temperature

Maximum BBU exhaust air temp shall not exceed 55C at back pressure between -0.05 to 0.05” H2O. While BBU is plugged in, the BBU fan(s) shall still function properly even at low/Standby load (FSC should increase fan speed if needed to overcome the high back pressure).

8. Mechanical

8.1. BBU Module Physical Dimensions

The BBU module size is 78.1mm x 87.6mm x 678.5mm [Width x Height x Depth]



8.2. Construction

The BBU base and cover shall be assembled using flathead screws. No rivets are allowed as the BBU must have the ability to be opened using a screwdriver. The individual base and cover can be welded, riveted or screwed together, consistent with meeting shock and vibration requirements. There shall be no sharp corners or edges.

8.3. Materials and Fasteners

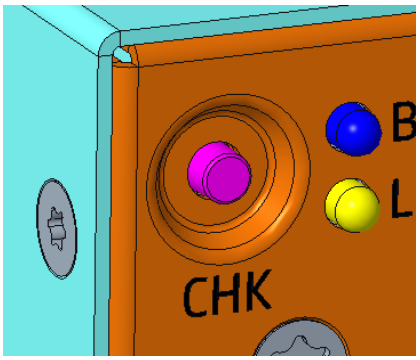
The sheet metal material shall be steel, pre-plated hot-dip zinc coated, with 1.0mm – 1.2mm of thickness unless otherwise specified. Any plastic material used should meet UL 94-V0 specifications. It is highly suggested to use PCR (post-consumer recycled) plastic. The following PCR plastics have been qualified for use:

- GLite MBS-200BKR01
- GLite MBS-200GNR01
- Kingfa JH960-6950 C2B-S0759
- Kingfa JH960-6950 C7G-S0023
- Wistron WAM NCT50T##

8.4. BBU Health Check Button

The BBU shall have a health check button in order to validate the functionality of the BBU module before insertion into the shelf. Button to be recessed so the top does not protrude past the front panel of the BBU in natural state. Recess shall have enough space for proper finger engagement. Suggested recess depth is 2mm.

When the health check button is pressed, BBU OK LED should light up solid blue for 10 seconds, indicating full functionality. If there is a fault, EOL, LOW V, or FAULT/LOC LEDs will light up solid amber for 10 seconds, indicating a failure. Please see Section 8.5 for further information regarding faults.



8.5. Indicators/LED

The front of the BBU shall display the following LEDs, single color or bicolor.

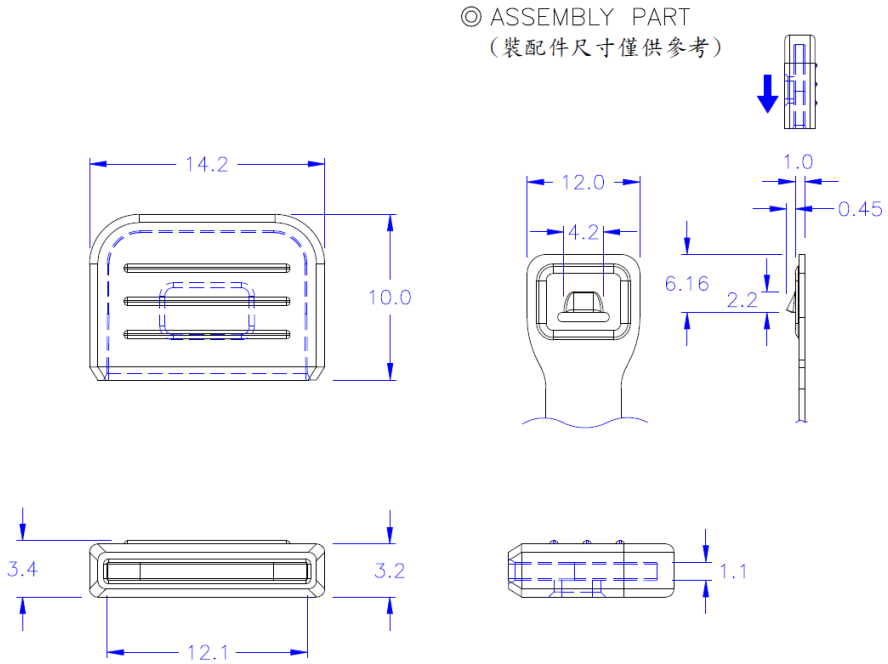
Silkscreen	Display	Color	Meaning
BBU OK		Solid Blue	BBU ready
		Blinking Blue @0.5s on/0.5s off	FW update mode
		Blinking Blue @1s on/1s off	Charging and not in FW update mode
		Off	Default
LOW V		Solid Amber	BBU low Capacity*
		Blinking Amber @0.5s on/0.5s off	BBU discharging

		Off	Default
EOL		Solid Amber	BBU EOL**
		Off	Default
FAULT/LOC		Solid Amber	Permanent fault (Replacement required)
		Blinking Amber @0.5s on/0.5s off	Recoverable temporary fault/Locate
		Off	Default

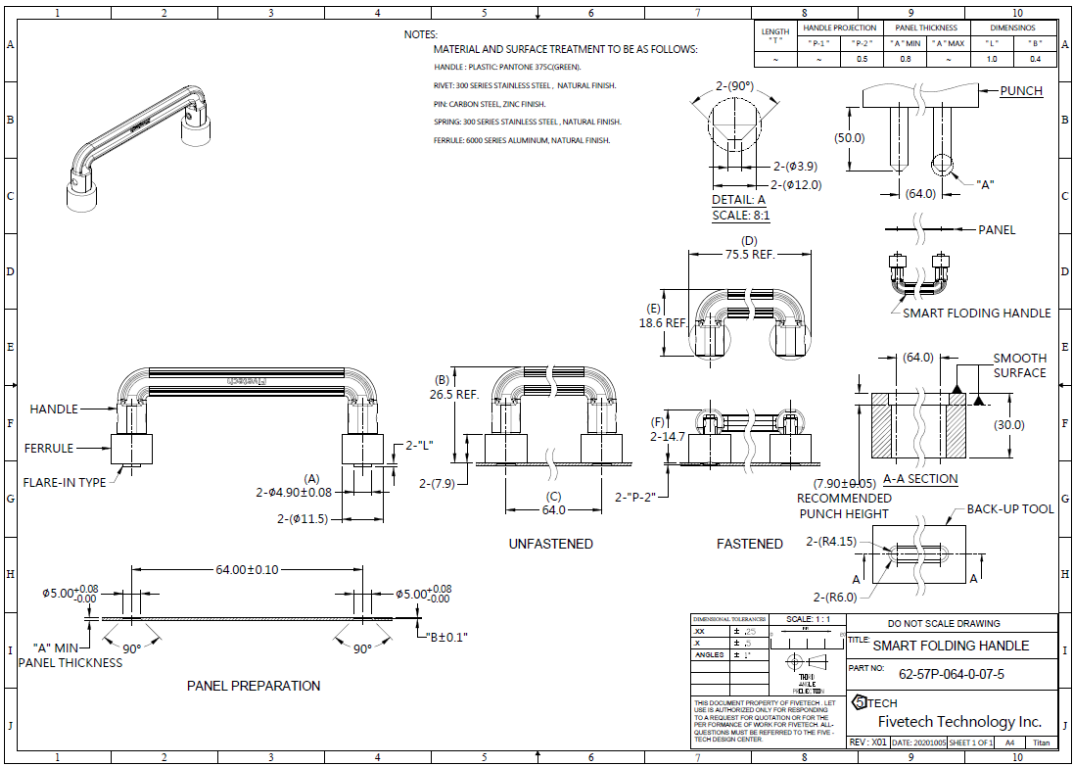
* Low V BBU SOC is below 30%.
** EOL threshold is defined based on BBU capacity degradation due to cell aging. When BBU FCC or SOH falls below EOL threshold, that means the BBU capacity at 3.9V PCM charge threshold is not able to support the full power ≥90s default backup time. The BBU must be able to support the described backup sequence at EoL (End of Life), at least 4 years of service at +35C ambient temperature, and with cells charged to 3.9V.
The EoL threshold shall be user programmable through a Modbus command according to the user programmable discharge time.

8.6. Latch and Handle Requirements

A latch and handle are required for BBU removal. The latch shall be attached in the location shown on the mechanical drawing, to interface with the cutout in the chassis. The latch design may vary, but the finger interface of the latch must be Pantone 375C (Green). It is suggested to use Pingood MHL-14JP-A9H3 as the plastic tab for the latch.



The handle shall be attached in the location shown on the mechanical drawing. This handle is flared into the BBU front panel sheet metal and shall only be folded 90° rightward. The handle shall not protrude past BBU right surface when folded. The handle design may vary, but it must be foldable and be Pantone 375C (Green) colored. It is suggested to use Fivetech 62-57P-064-0-01-0 for the handle. Please note that the BBU will be heavy and the handle should be sturdy enough to carry the entire weight of the BBU.



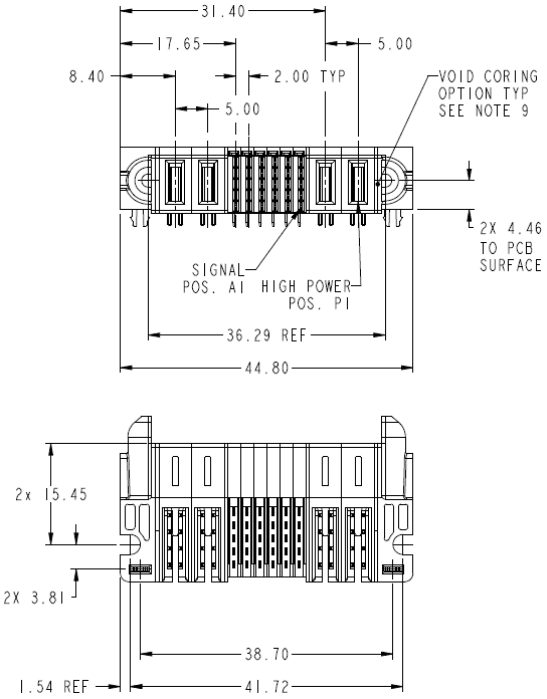
8.7. Chassis Interface

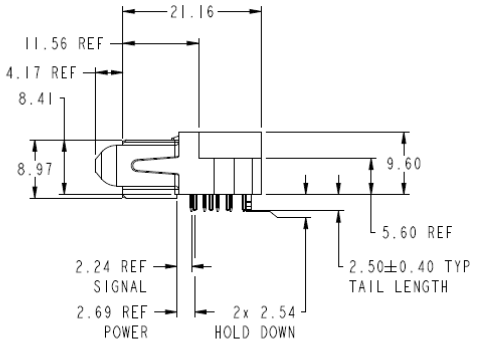
The handle of the BBU may not protrude from the front surface of the BBU by more than 25mm. The latch shall be located on the top side of the BBU and interface with a rectangular cutout in the chassis wall (please refer to the 3D drawing for latch location on the BBU. They should only lock into place when a good electrical contact is made on the rear blind mate connectors. This scheme will allow a quick installation of the BBU in the tray, and without the need of using a screwdriver.

8.8. Rear Blind Mate Connector

The rear blind mate connector of the BBU shall be Amphenol 10127401-03H1510LF or equivalent. This is a PwrBlade ULTRA HD connector with 4 high power pins, 30 signal pins. Please refer to the drawing for more details.

The connector position within the BBU is fixed in X, Y, and Z direction according to the 3D drawing. This cannot be altered due to mix-and-match requirements for the BBUs into the shelf.





8.9. Rear Blind Mate Connector Protection

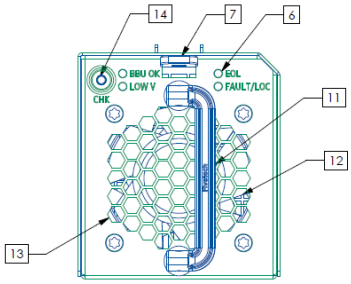
A method of protecting the rear blind made connector on the BBU module is required to prevent damage from accidental mishandling during manufacturing or end user handling of the module. Please review mechanical 3D CAD for reference design of protection brackets. These brackets should not interfere with any features on the BBU Shelf.

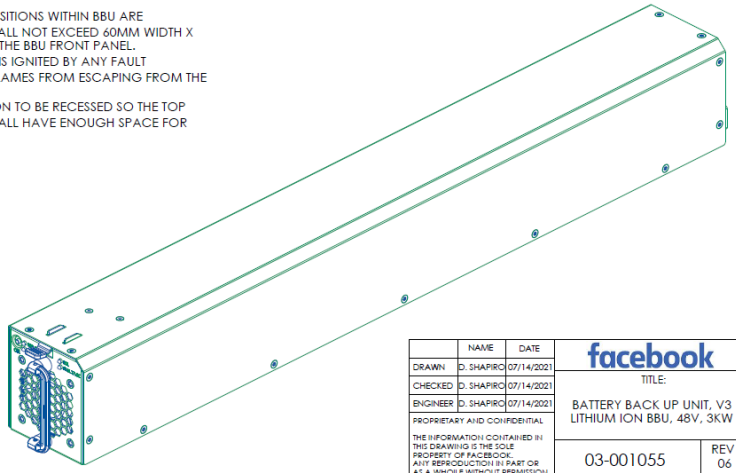
8.10. Mechanical Drawings

NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-2009.
2. ALL DIMENSIONS ARE IN MM.
3. ALL COMPONENTS SHALL BE UL 94V-0 RECOGNIZED AND ROHS COMPLIANT.
4. CASE MATERIAL SHALL RESIST THE CREATION OF ZINC WHISKERS, SUCH AS ASTM A653 AND JISG3302 SGCC.
5. ALL DIMENSIONS ARE CONSIDERED CRITICAL TO FUNCTION DIMENSIONS AND SHALL BE INCLUDED IN PART QUALIFICATION.
6. LEDS SHALL FOLLOW FACEBOOK INDICATOR SPEC. LEDS TO BE LABELED IN A PERMANENT AND LEGIBLE MANNER LOCATED APPROXIMATELY WHERE SHOWN. TEXT 2.5 MM TALL MINIMUM.
7. LATCH TAB COLOR PANTONE 375C GREEN OR SIMILAR WITH FACEBOOK ENGINEERING WRITTEN APPROVAL. LATCH TAB MPN: PINGOOD MHL-14JP-A9H3 OR EQUIVALENT. LATCHES MUST HAVE A BACKSTOP TO PREVENT DAMAGE TO LATCH DURING ACTUATION.
8. AIRFLOW PER INDICATED DIRECTION
9. ALL EDGES SHALL BE CONDITIONED FOR HANDLING WITH INDUSTRY STANDARD BURR NO LARGER THAN 10% OF MATERIAL THICKNESS AND SHALL CONFORM TO UL SAFETY SPECIFICATION 1349.
10. ALL COMPONENTS SHALL BE CLEAN AND FREE OF RUST AND FOREIGN MATERIAL SUCH AS DIRT, OIL, GREASE, OR OTHER CONTAMINANTS.
11. BBU HANDLE IS A 90° FOLDABLE HANDLE. THIS HANDLE IS FLARED INTO THE BBU FRONT SHEET METAL PANEL AND SHALL ONLY BE FOLDED 90° RIGHTWARD. THE HANDLE SHALL NOT PROTRUDE BBU RIGHT SURFACE WHEN FOLDED. MPN: FIVETECH 62-57P-064-0-07-5 OR EQUIVALENT.
12. ONE FAN TO BE INSTALLED ON THE FRONT PORTION OF THE BBU. OTHER FAN POSITIONS WITHIN BBU ARE ACCEPTABLE WITH FACEBOOK ENGIENERING WRITTEN APPROVAL. THE FAN SIZE SHALL NOT EXCEED 60MM WIDTH X 60MM HEIGHT X 38MM THICKNESS. PERFORATION FOR THE FAN SHALL BE MADE ON THE BBU FRONT PANEL.
13. ENCLOSURE OPENINGS SHALL NOT NEGATIVELY AFFECT THE SAFETY WHEN FIRE IS IGNITED BY ANY FAULT CONDITION INSIDE THE ENCLOSURE. ENCLOSURE SHALL BE DESIGNED TO SUPRESS FLAMES FROM ESCAPING FROM THE FRONT OR REAR. REFERENCE UL9540A FOR TESTING CONDITIONS.
14. BBU HEALTH CHECK BUTTON TO BE PLACED IN APPROXIMATE LOCATION. BUTTON TO BE RECESSED SO THE TOP DOES NOT PROTRUDE PAST THE FRONT PANEL OF BBU IN NATURAL STATE. RECESS SHALL HAVE ENOUGH SPACE FOR PROPER FINGER ENGAGEMENT.

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	1	INITIAL RELEASE	11/18/2020	CX
	2	ADJUST LATCH MAX PROTRUSION	12/10/2020	CX
	3	UPDATE LATCH TAB, TORX SCREWS, REAR FLANGES,	01/27/2021	D. SHAPIRO
	4	UPDATED CONNECTOR TABS, EMI GASKET, HEALTH BUTTON	07/14/2021	D. SHAPIRO
	5	UPDATED PN	12/07/2021	D.SHAPIRO
	6	REMOVED EMI GASKET	09/12/2023	D.SHAPIRO





	NAME	DATE
DRAWN	D. SHAPIRO	07/14/2021
CHECKED	D. SHAPIRO	07/14/2021
ENGINEER	D. SHAPIRO	07/14/2021

PROPRIETARY AND CONFIDENTIAL

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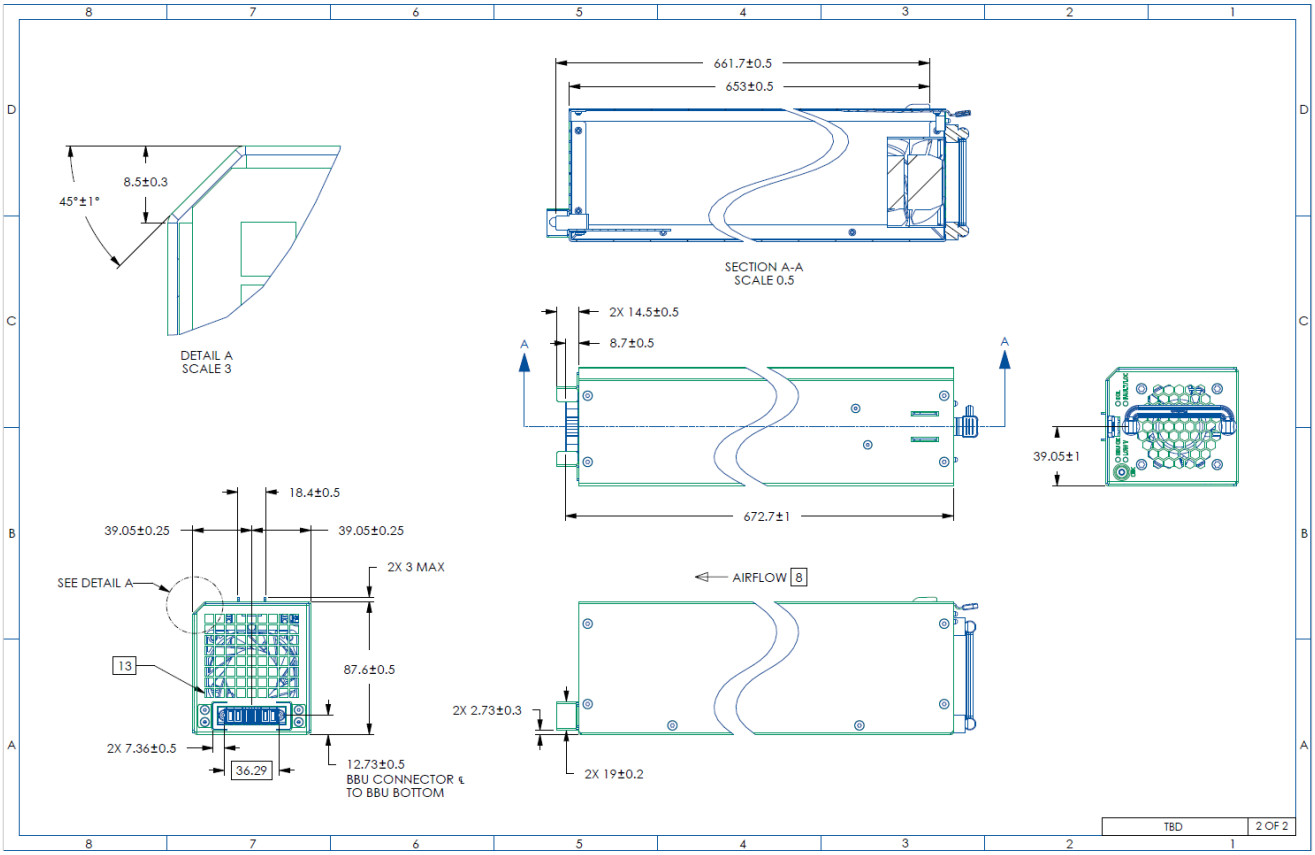
TITLE:

BATTERY BACK UP UNIT, V3
LITHIUM ION BBU, 48V, 3KW

03-001055 | REV 06

THIRD PROJECTION | 1 OF 2



9. Reliability and Quality

9.1. Derating Design

A comprehensive stress analysis and derating design shall be performed for the BBU. The stress analysis shall include electrical, thermal, and mechanical stresses with actual measurements. The components in the BBU design (excluding battery) shall be properly derated and to meet the derating guideline as specified in IPC-9592B “Requirements for Power Conversion Devices for the Computer and Telecommunication Industries”, Appendix A.

9.2. Reliability Prediction

A reliability prediction shall be performed for the BBU (excluding battery) using Telcordia SR-332 Issue 4 Method I, Case 3 (Parts Stress). The target MTBF for the BBU (excluding battery) shall be minimum 1,000,000 hrs at 45C, 100% load.

9.3. Design Failure Mode and Effect Analysis (DFMEA)

A comprehensive DFMEA shall be performed for the BBU. The DFMEA report shall include a list of critical components, risk areas, and corrective actions taken.

9.4. Burn-In (BI) and Ongoing Reliability Testing (ORT)

Burn-in and ORT shall be performed particularly on the DC-DC converter of the BBU using IPC9592B guidelines and/or procedures or supplier may propose a burn-in and ORT scheme for META review and approval.

9.5. Manufacturing Quality

It is required to meet the quality process requirements as specified in IPC-9592B, Section 6 (“Quality Process”), which include PFMEA, statistical process control (SPC), corrective action process, yield control, materials traceability, product change notice (PCN), qualification of change, etc.

9.6 E-cap life

All e-caps must meet e-cap life of >8 years.

10. Compliance requirements

The BBU shall be designed for compliance to allow worldwide deployment. Additionally, the manufacturer is fully responsible for:

- ensuring the complete compliance of the BBU shelf in the environment it is intended to function (as described by the Rack Spec)
- maintaining and updating the BBU shelf safety reports to current requirements and all newly released requirements.
- all design and recertification costs required to update the BBU to meet the new
- requirements.
- Meeting EMC requirements
- Meeting Safety requirements

The manufacturer is responsible for obtaining the safety certifications specified below.

10.1. Safety Standards

The product is to be designed to comply with the latest edition, revision, and amendment of the following standards. The product shall be designed such that the end user could obtain the safety certifications: UL 62368-1, IEC 62368-1 and EN 62368-1; hazard-based performance standard for Audio video, IT & Communication Technology Equipment

The manufacturer shall obtain the following safety certifications for the BBU shelf as applicable. Only requirements that absolutely rely on or are affected by the system may be left to the system level evaluation [i.e. minimize Conditions of Acceptability]. Below are common requirements for North America and Europe. For other countries, different certifications may be required:

- UL or an equivalent NRTL for the US with follow-up service (e.g. UL or CSA)
- CB Certificate and test report issued by CSA, UL, VDE, TUV or DEMKO
- CE Marking for EU
- UL1973 (Recog) cRUus
- IEC62133
- IEC62619
- 62368-1 (UL/IEC)
- UN38.3
- UL9540
- UL9540A for BBU cell, BBU module and unit

10.1.1 Component Safety requirements

Following are the safety requirements for major components:

- All Fans shall have the minimum certifications: UL and TUV or VDE.
- All current limiting devices shall have UL and TUV or VDE certifications and shall be suitable rated for the application where the device in its application complies with IEC/UL 62368-1.

- All printed wiring boards shall be rated UL94V-0 and be sourced from a UL approved printed wiring board manufacturer.
- All connectors shall be UL recognized and have a UL flame rating of UL94V-0.
- All wiring harnesses shall be sourced from a UL approved wiring harness manufacturer. SELV Cable to be rated minimum 80V, 130C.
- Product safety label must be printed on UL approved label stock and printer ribbon. Alternatively, labels can be purchased from a UL approved label manufacturer.
- The product must be marked with the correct regulatory markings to support the certifications that are specified in this document.
- Battery cell shall comply with applicable safety standards including UL9540
- BBU module shall not explode or spread fire when battery cells undergo thermal runaway condition.
- BBU shelf shall not explode or spread fire when battery module undergoes thermal runaway condition.

10.2. EMC Requirements

The BBU shall meet the following requirements in the latest edition of standards when operating under typical load conditions and with all ports fully loaded.

The BBU integrated into the shelf is called the component BBU. Manufacturer shall provide the proof of compliance for the component BBU that are required for spare parts shipment. The component BBU shall not contribute any noncompliant conditions to the end-use product.
If at any time it is found that a supplier's component BBU causes the end-use product to fail emissions and/or immunity testing, the supplier will be instructed to investigate and resolve the problem.
The BBU shelf shall have minimum 6dB margin from the Class A limit for the radiated and conducted emissions. Depending on the system manufacturer's design goals and business needs, more margin may be required when it is integrated into the final end system.
The following EMC Standards (the latest version) are applicable to the product.

- FCC /ICES-003
- CISPR 32/EN55032
- CISPR 35/EN55035 - Immunity
- EN61000-3-2 – Harmonics (Test with power shelf integrated)
- EN61000-3-3 - Voltage Flicker (Test with power shelf integrated)

Each individual basic standard for immunity test has the following minimum passing requirement. Higher level of passing criteria may be applied depending on the system manufacturer's design goals and business needs.

- EN61000-4-2 Electrostatic Discharge Immunity
  - Contact discharge: >5.6kV
  - Air discharge: >11.2kV
- EN61000-4-3 Radiated Immunity
  - > 3V/m
- EN61000-4-4 Electrical Fast Transient Immunity
  - AC Power Line: >1kV
  - Signal Line: >0.5kV
- EN61000-4-5 Surge
  - AC Power Line: >1kV (Line-to-line), >2kV (Line-to-earth)
  - Signal Port: >1kV
- EN61000-4-6 Immunity to Conducted Disturbances
  - DC Power Line: > 3Vrms
- EN61000-4-8 Power Frequency Magnetic Field Immunity, when applicable
  - > 1A/m
- EN61000-4-11 Voltage dip and sag

10.3. Environmental Compliance

The BBU shelf (including all components inside) shall comply with the following minimum environmental requirement and manufacturer shall provide full material disclosure, Declaration of Conformity and technical documentations to demonstrate compliance. The system manufacturer may have additional requirements depending on its design goals and business needs.

- RoHS Directive (2011/65/EU and 2015/863/EU); aims to reduce the environmental impact of EEE by restricting the use of certain substances during manufacture
- REACH Regulation (EC) No 1907/2006; registration with the European Chemicals Agency (ECHA), evaluation, authorization and restriction of chemicals.
- Halogen Free: IEC 61249-2-21, Definition of Halogen Free, 900ppm for Br or Cl, or 1500ppm combined
- US SEC conflict mineral regulation to source mineral materials from socially responsible countries, if applicable
- Waste Electrical and Electronic Equipment ("**WEEE**") Directive (2012/19/EU) if applicable; aims to reduce the environmental impact of EEE by restricting the use of certain substances during manufacture

10.4. Documentation

The manufacturer shall provide reproducible copies of all pertinent documentation relating to the following:

- Product Information
- Schematics, PCB layout artwork and bill of material including key component specifications at each design phase
- Functional test report at each design phase
- Applicable compliance reports, certifications and declaration of conformance.
- Other applicable certificates required by the system manufacturer.

Reference Documents

ORV3 PMI Specification

ORV3 BBU Shelf Specification

ORV3 PSU Specification

ORV3 PSU Register map

ORV3 Power Shelf Specification

ORV3 BBU Register Map

ORV3 Modbus Communication Specification

ORV3 BBU CAN Bus Communication Specification

ORV3 BBU Modbus Writable Description

Appendix A - Checklist for IC approval of this Specification (to be completed by contributor(s) of this Spec)

Complete all the checklist items in the table with links to the section where it is described in this spec or an external document .

Item	Status or Details	Link to detailed explanation
Is this contribution entered into the OCP Contribution Portal?	Yes	If no, please state reason.
Was it approved in the OCP Contribution Portal?	Yes	If no, please state reason.
Is there a Supplier(s) that is building a product based on this Spec? (Supplier must be an OCP Solution Provider)	Yes	List Supplier Name(s) Delta
Will Supplier(s) have the product available for GENERAL AVAILABILITY within 120 days?	No	If more time is required, please state the timeline and reason for extension request. Please have each Supplier fill out Appendix B.